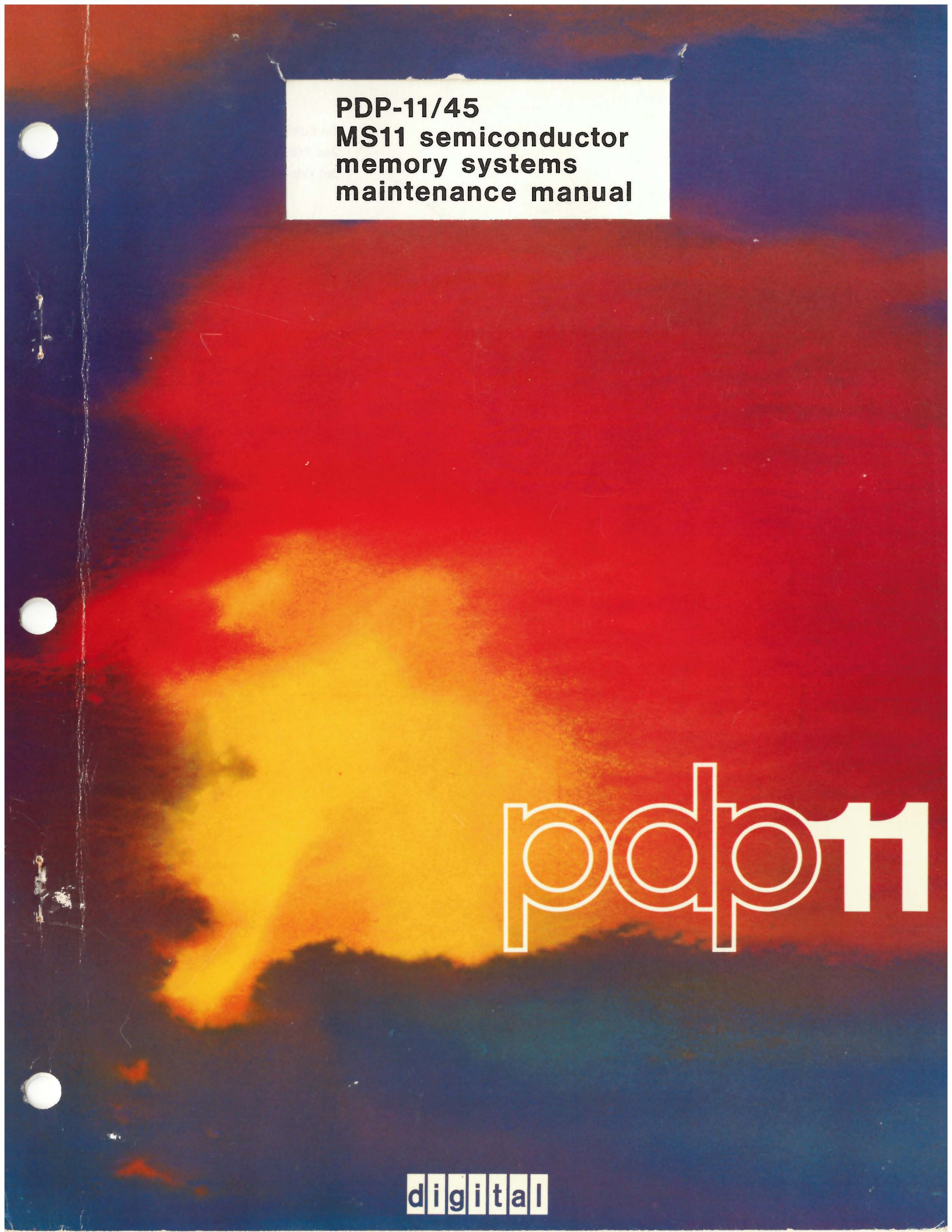
PDP-11/45
MS11 semiconductor memory systems maintenance manual



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PDP-11/45
MS11 semiconductor memory systems maintenance manual

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INTRODUCTION

This manual describes the MS11 options that constitute the PDP-11/45 Semiconductor Memory System. Its primary purpose is to provide information for DEC Field Service representatives and customer personnel, with similar PDP-11/45 training, to perform on-site maintenance of the MS11 options. The information is presented in four chapters.

Chapter 1 describes the MS11 Semiconductor Memory System structure. It also provides module specifications and system configuration information.

Chapter 2 describes semiconductor memory system access operations, interfacing, and addressing.

Chapter 3 provides a detailed analysis of semiconductor memory logic operation.

Chapter 4 presents the procedures required for semiconductor memory calibration and maintenance.

All descriptions assume that the reader is familiar with basic digital computer theory and the operating characteristics of bipolar and metal-oxide semiconductor (MOS) digital integrated circuits. Because of the many recent advances in MOS technology concerning memory system applications, Appendix A contains a description of MOS memory circuit theory.

Data, address, and control signals relevant to semiconductor memory operation are transmitted on the Unibus or the PDP-11/45 Fastbus. This manual references the data, address, and control lines that interface the semiconductor memory system with other PDP-11/45 units, according to the conventions established for Unibus and PDP-11/45 signal mnemonics. For example, SAPJ PA ⟨17:06⟩ H refers to the 12 physical-address (PA) inputs, named PA17 through PA06, which are generated as shown on drawing SAPJ. The prefix SAPJ indicates sheet J of the SAP module schematic. Complete details on data, address, and control signal origin and derivation are provided in the following related manuals:

PDP-11/45 System Maintenance Manual	DEC-11-H45B-D
KB11 Central Processor Maintenance Manual	DEC-11-HKBB-D
KT11 Memory Management Unit Maintenance Manual	DEC-11-HKTB-D
PDP-11 Unibus Interface Manual (Second Edition)	DEC-11-HIAB-D

CHAPTER 1
SYSTEM DESCRIPTION

1.1 INTRODUCTION

Digital Equipment Corporation's MS11 Semiconductor Memory Systems for the PDP-11/45 System are high-speed random-access memories available in two basic solid-state types: bipolar (TTL) and metal-oxide semiconductor (MOS). The distinction between bipolar and MOS memory systems is made in the specific MSI components used to form the memory storage matrices. Both forms of semiconductor memory matrices operate under the control of the M8110 Semiconductor Memory Control module. The M8110 can control either four 1024-word M8111 Bipolar Memory Matrix modules or four 4096-word G401 MOS Memory Matrix modules (Figure 1-1). One bipolar memory system provides storage for 4096 16-bit words, and one MOS memory system provides storage for 16,384 16-bit words. Both forms of semiconductor memory are available with or without byte parity.

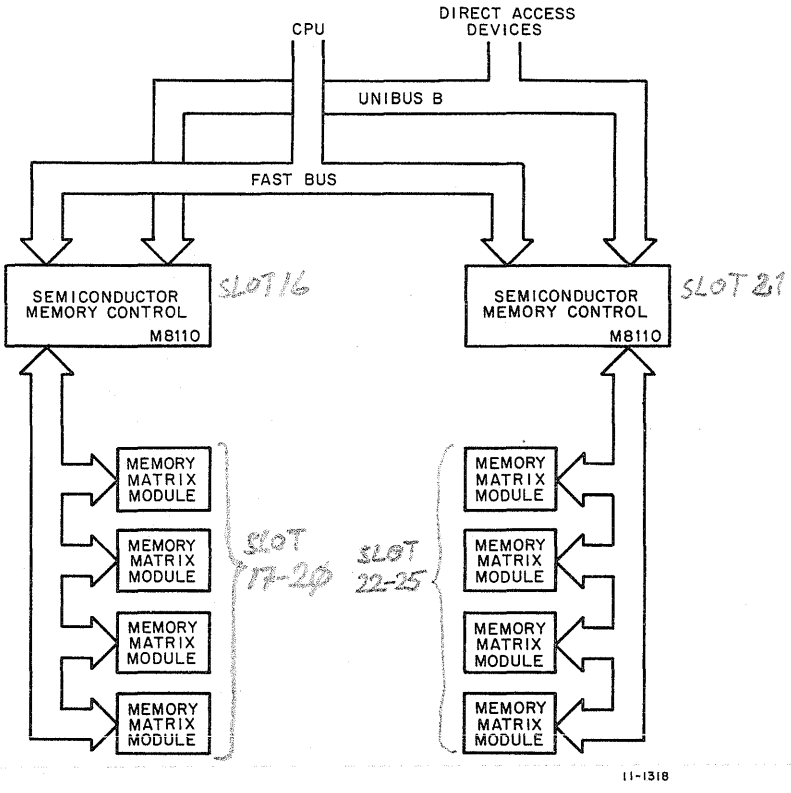


Figure 1-1 MS11 Semiconductor Memory System, Block Diagram

The bipolar and MOS semiconductor memories can be jointly or separately operated from either the KB11 Fastbus or the PDP-11 Unibus, or from both, depending on the specific PDP-11/45 System configuration. When operated from the Unibus, each semiconductor memory system functions as a PDP-11 compatible peripheral and can serve as the basic memory in a large-scale system. Operation under joint control of the Fastbus and Unibus provides direct high-speed memory access through the Fastbus for the KB11 Processor, while maintaining the processor/peripheral relationships characteristic of the Unibus. Whether operating jointly or separately with the Unibus and/or Fastbus, a semiconductor memory always assumes the role of a "slave" device to the processor. Under Unibus control, the memory also is "slave" to any peripheral (direct access) device currently designated "master".

Because readout from semiconductor memories is non-destructive, the write-after-read-cycle time associated with ferrite-core memories is eliminated. In addition, the switching speed for semiconductor memories is characteristically much faster than that for the ferrite-core memory. The extremely high switching speeds characteristic of bipolar memory cells permit memory cycle times of 300 ns for an operating bipolar memory system. MOS semiconductor memory systems have slower cycle times of 450 ns.

1.2 M8111 BIPOLAR MEMORY MATRIX MODULE

The M8111 Bipolar Memory Matrix module is an 8-1/2 in. X 15 in. multilayer glass hex board, configured to either store or not store byte parity. The M8111YA parity-equipped modules contain seventy-two 256 X 1-bit TTL MSI memory circuits, interconnected to form a 1024 X 18-bit memory matrix. Each 18-bit word in this matrix is formed by two 8-bit bytes and two parity bits, one per byte. This module also contains appropriate address decoding and driving logic, 18 write-data inversion stages, and control-signal decoding logic. All decoding inversion and driving logic is formed by TTL integrated circuits. Address lines ⟨14:11⟩ at each M8111 matrix module are jumper-connected so that in a given bipolar memory system each matrix module can be configured to decode a unique address. The M8111 Bipolar Memory Matrix module is identical to the M8111YA in all respects, except that the M8111 contains sixty-four 256 X 1-bit MSI memory circuits, interconnected to form a 1024 X 16-bit memory matrix without byte parity.

1.3 G401 MOS MEMORY MATRIX MODULE

The G401 MOS Memory Matrix module is an 8-1/2 in. X 15 in. double-sided, multilayer glass hex circuit board, also configured to either store or not store byte parity. The G401YA parity-equipped module contains seventy-two 1024 X 1-bit MOS MSI circuits, interconnected to form a 4096 X 18-bit memory. The 18-bit word configuration is exactly the same as the bipolar matrix, i.e., two 8-bit bytes and two parity bits, one per byte. This module also contains appropriate logic to level-shift addresses, data, and control signals from TTL to MOS and MOS to TTL voltage levels; and 16 or 18 intergrated-circuit sense amplifiers, depending on whether parity is specified, one for each of the read-sense lines. The states of memory address (MAD) register bits ⟨02:01⟩ and ⟨14:13⟩ are decoded at this module to select the specific module and the group of 1024 words addressed within the selected module. Address bits MAD ⟨14:13⟩ are jumper-connected so that each 4096-word matrix can be selected and wired for a unique address assignment. The G401 MOS Memory Matrix module is identical in all respects to the G401YA, except that the G401 contains sixty-four 1024 X 1-bit MSI memory circuits, interconnected to form a 4096 X 16-bit memory matrix without byte parity.

Operation of the MOS memory matrix is substantially different from the bipolar matrix in two respects. First, because of the nature of the dynamic MOS storage cell (Appendix A), each memory access must include a time interval for precharging the addressed cells prior to the actual access. Second, all memory locations in an MOS system must be periodically refreshed, usually every 1 ms, to assure data validity during any extended standby intervals.

1.4 M8110 SEMICONDUCTOR MEMORY CONTROL MODULE

The M8110 Semiconductor Memory Control module is a fully integrated two-port memory controller capable of controlling either four M8111 or four G401 matrix modules. A simplified block diagram of the M8110 control is shown in Figure 1-2. The M8110 control multiplexes memory access addresses and associated data between the PDP-11/45 Fastbus and a Unibus, and directs logic and timing sequences necessary for the storage or retrieval of each data word or byte associated with a given access cycle. Each of the M8110 control functions is described briefly in the following paragraphs.

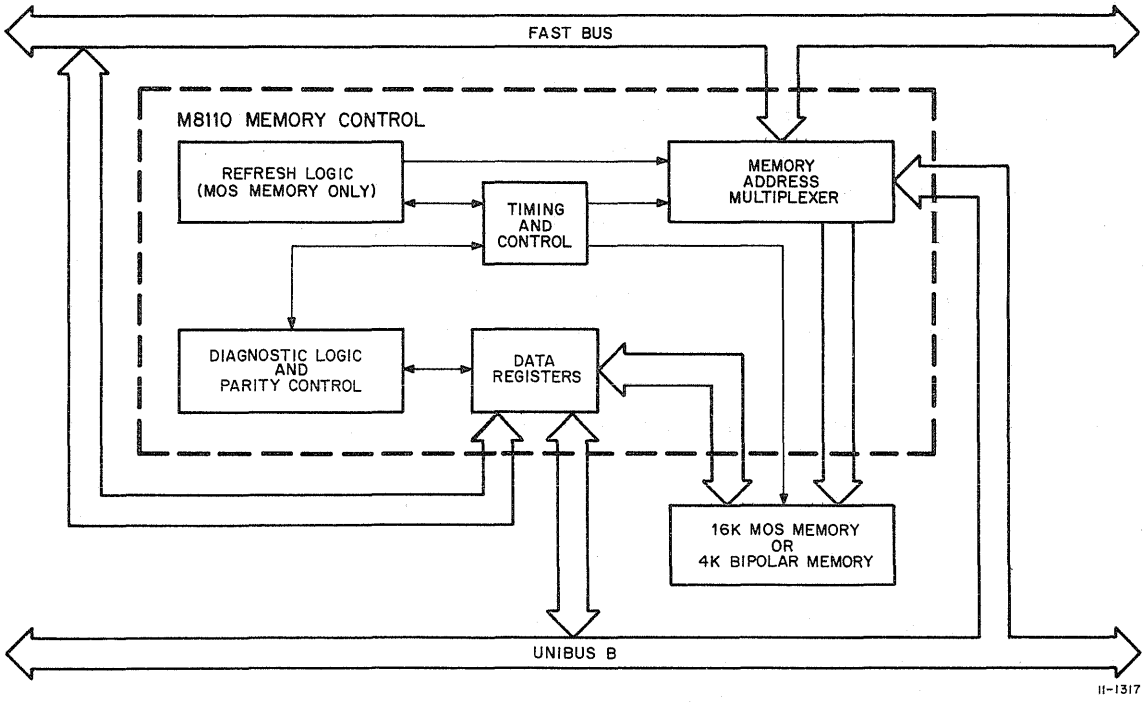


Figure 1-2 MS11 Semiconductor Memory Control Module, Block Diagram

1.4.1 Memory Address Multiplexing

The memory address multiplexing function involves two sequential actions under direct control of the M8110 timing and control logic. First, based on priority, arbitration of memory access requests performed by the timing and control logic, Fastbus, Unibus, or refresh addresses (for MOS memory systems only) are multiplexed into the memory address (MAD) register. Second, through a parallel bit-to-bit connection scheme, Fastbus or Unibus addresses are mapped into the MAD register. Once mapped into the MAD register, and address is strobed into the associated bipolar or MOS memory matrix module selected by that address through action of the M8110 timing and control function.

1.4.2 Write and Read Data Registers

The M8110 contains two data registers: the write-data (DATO) register, and the read-data (DATI) register. The DATO register multiplexes a 16-bit data word (or two 8-bit data bytes), from either the Fastbus or Unibus, and stores that data until strobed into the associated bipolar or MOS memory matrix module by the M8110. The 18-bit DATO register stores parity for the lower and upper data bytes in the most significant DATO register stages. These parity bits are generated as part of word or byte storage in the DATO register. Data from the

Unibus is received at the M8110 Unibus interface for storage in the DATO register. Fastbus data to be written is received directly at the DATO register because of the proximity of the M8110 to the KB11 Processor. At the appropriate time, the data accompanying a DATO cycle is strobed into the memory location designated by the associated address.

The M8110 DATI register receives and stores data from the location addressed in the memory matrix as a direct result of a Unibus or Fastbus DATI cycle. At the end of a DATI cycle, data is strobed jointly onto the M8110 Unibus interface, and to the Fastbus for retrieval by the requesting bus. Fastbus data lines are unidirectional, Unibus data lines are bidirectional.

1.4.3 Timing and Control

The M8110 timing and control interprets control signals from the Fastbus or Unibus and derives the internal multiplexing priorities, timing, and the nature of the operation to be subsequently performed (DATO or DATI). In addition, specific portions of the address contained in the MAD register are decoded by the selection logic to identify the physical memory selected, the memory section to be addressed (one out of four 1024-word sections or one out of four 4096-word sections), the required byte configuration, and to determine if data words are to be interleaved. If the operation to be performed is a DATO, the timing and control logic develops the strobe levels necessary to load multiplex addresses and data, according to the priority of the request, into pertinent registers. The timing and control logic also enables the designated memory section for writing and performs the DATO operation.

Because readout from semiconductor memories is non-destructive, the timing and control logic strobes the addressed data onto the output lines which connect to both buses. In this case, the bus that initiated the read operation receives the data at the bus input as the data requested.

1.4.4 Refresh Logic

The nature of the dynamic MOS MSI circuits forming the G401 MOS Memory Matrix module requires that each storage cell, which is the circuit equivalent of a capacitive node, be periodically charged above the threshold of the data stored. Refreshing the data contained in each integrated-circuit memory requires that all states of the row address for that circuit be cycled each 1 ms. The M8110 refresh logic performs this function automatically by generating 32 sequential row addresses during each 1-ms period. These sequential addresses are then input to the address multiplexer. Coincident control levels from the refresh logic serve to enable the address priority portion of the timing and control logic to permit input of refresh addresses at the assigned priority level.

Each DATO or DATI operation (with the exception of the write portion of a write-after-read operation) also includes the precharging or refreshing of each address written into or read. When the M8110 is used with bipolar memory matrix modules, this refresh logic is inhibited and the precharge interval is ignored.

1.4.5 Parity Control

Data to be written is transferred to the M8110 over 16 data lines. If the operation is a DATO cycle, parity is generated and stored in bit 16 for the low-order byte and in bit 17 for the high-order byte. If the operation is a DATOB, parity is generated only for the byte written and stored in the corresponding parity.

During DATI operations, parity is checked after each 16 bits of data read are transferred to the M8110 output data register. If a parity error is detected, the respondent bus is notified.

1.4.6 Diagnostic Logic

M8110 memory control diagnostic logic allows writing of data from the Unibus with parity selected as odd or even in any memory address, and to check the parity generated for odd or even, regardless of the manner generated. Part of the M8110 memory control diagnostic logic structure decodes specific Unibus addresses that are jumper-connected at each M8110 so that each half of the total semiconductor memory has a unique address. Each control also contains two diagnostic parity registers that are selected by M8110 interpretation of Unibus control signals to select one of these two registers for loading of Unibus data within a DATO cycle. The data loaded is then interpreted to determine the specific section of memory designated for diagnostic parity exercising. In this manner, diagnostic software can selectively exercise designated semiconductor memory areas for parity, while protecting those memory areas occupied by the diagnostic programs. Each M8110 diagnostic parity register can also be selectively read through execution of a Unibus DATI cycle. Parity error indication, when enabled, is transmitted directly to the processor through the Fastbus.

1.5 SYSTEM SPECIFICATIONS

Characteristics	M8110 Semiconductor Memory Control Module	M811 Bipolar Memory Matrix Module	G401 MOS Memory Matrix Module
Storage Capacity	NA	1024 18-bit words	4096 18-bit words
Maximum Access Time:			
DATO cycle	NA	NA	NA
DATI cycle	NA	200 ns	350 ns
Maximum Cycle Time	NA	300 ns	450 ns
Operating Voltages:			
VCC	+5V, -15V	+5V	±5V
VBB			+23.7V
VDD			+0.7V
VSS			+19.7V
Over-Voltage Regulation	±5%	±5%	±5%
*Maximum Power Consumption:			
active	19.65W	50W	39.35W
inactive	19.65W	50W	16.01W
Environmental conditions:			
temperature	32° to 120°F (0° to 48°C)	32° to 120°F (0° to 48°C)	32° to 120°F (0° to 48°C)
humidity	10% to 80%	10% to 80%	10% to 80%
Mechanical Parameters:			
height	15 in. (38.1 cm)	15 in. (38.1 cm)	15 in. (38.1 cm)
width	8.5 in. (21.59 cm)	8.5 in. (21.59 cm)	8.5 in. (21.59 cm)
depth	1/2 in. (1.27 cm)	1/2 in. (1.27 cm)	1/2 in. (1.27 cm)
Construction	fiberglass/ multilayer	fiberglass/ multilayer	fiberglass/ multilayer
Cooling	internal fan	internal fan	internal fan
Mounting	dedicated plug-in slot in CPU	dedicated plug-in slot in CPU	dedicated plug-in slot in CPU

* Maximum power per module of each type.

1.6 SEMICONDUCTOR MEMORY SYSTEM CONFIGURATIONS

Tables 1-1 and 1-2 list the quantity of options that are required as a result of the selected memory type (MOS or bipolar) and size. The module complement that comprises the corresponding option is also shown. If, for example, a 24K capacity MOS memory without parity is desired, the required configuration will consists of one MS11-BC option (composed of one M8110 module, one H746A module, and one H744A module), one MS11-BD option, and six MS11-BM options (G401 memory matrices). The additional M8110 Controller (MS11-BD option) is necessary for the 8K of memory in excess of the 16K controlled by the MS11-BC option.

Table 1-1
MOS Memory System Configuration

Memory Capacity Option		Option Type Number			
		MS11-BC	MS11-BD	MS11-BM	MS11-BP
		Module Complement			
With Parity	Without Parity	(1)M8110 (1)H746A (1)H744A	(1)M8110	(1)G401	(1) G401YA
4K		1			1
	4K	1		1	
8K		1			2
	8K	1		2	
12K		1			3
	12K	1		3	
16K		1			4
	16K	1		4	
20K		1	1		5
	20K	1	1	5	
24K		1	1		6
	24K	1	1	6	
28K		1	1		7
	28K	1	1	7	
32K		1	1		8
	32K	1	1	8	

Table 1-2
Bipolar Memory System Configuration

Memory Capacity Option		Option Type Number		
		MS11-CC	MS11-CM	MS11-CP
		Module Complement		
With Parity	Without Parity	(1)M8110 (2)H744A	(1)M8111	(1)M8111YA
1K		1		1
	1K	1	1	
2K		1		2
	2K	1	2	
3K		1		3
	3K	1	3	

(continued on next page)

Table 1-2 (Cont)

Bipolar Memory System Configuration

Memory Capacity Option		Option Type Number		
		MS11-CC	MS11-CM	MS11-CP
		Module Complement		
With Parity	Without Parity	(1)M8110 (1)H744A	(1)M8111	(1)M8111YA
4K		1		4
	4K	1	4	
5K		2		5
	5K	2	5	
6K		2		6
	6K	2	6	
7K		2		7
	7K	2	7	
8K		2		8
	8K	2	8	

CHAPTER 2
MEMORY SYSTEM INTERFACE OPERATIONS

2.1 INTRODUCTION

A PDP-11/45 System can be equipped with one or two M8110 Semiconductor Memory Control modules. Each M8110 module, in turn, can exercise control of up to four M8111 Bipolar Memory Matrix modules, or up to four G401 MOS Memory Matrix modules. Since the memory capacity of these two matrix module types is different (the M8111 provides 1K and the G401 4K of memory) the total memory capacity available to the user is determined by the selected configuration. A typical two-M8110 module arrangement can consist of up to 8K of bipolar memory in 1K increments or up to 32K of MOS memory in 4K increments. The two-controller configuration might also have one of the controllers directing bipolar matrices while the other is connected to MOS matrices. However, memory matrices of different types can not be connected to the same M8110 control. As indicated in Tables 1-1 and 1-2, the memory capacity determines the number of M8110 modules required (the maximum configuration is 4K of bipolar or 16K of MOS memory per module). Figure 2-1 illustrates the memory system, bus, and processor relationship. Within a PDP-11/45 computer system, the CPU communicates with associated semiconductor memory controls through an extremely high-speed information path which is internal to the CPU and under control of the CPU Fastbus. One Unibus in the system, normally Unibus A, also communicates with the two M8110 controls.

Each M8110 control, in turn, communicates with up to four bipolar or four MOS memory matrix modules. Therefore, an operating M8110 Semiconductor Memory Control has three active interfaces: the Fastbus interface, the Unibus interface, and the memory bus. The relationship of a typical PDP-11/45 Semiconductor Memory System to these interfaces is shown in Figure 2-2. Because the M8110 control and associated memory matrix modules are physically located in the PDP-11/45 processor, connection to the Fastbus is by direct-wiring the control and matrix module connectors to the PDP-11/45 CPU backplane. However, the potentially remote location of a second Unibus, with respect to the M8110 control, requires a defined Unibus interface on the control to drive and receive information and control signals to and from that Unibus. Like the Fastbus connection, memory bus connection between an M8110 control and associated M8111 bipolar or G401 MOS memory modules involves physically adjacent connectors, so that control-matrix module information and signals are direct-wire connected.

Discussion of semiconductor memory system interfaces will involve a description of memory access operation, a definition of each interface in terms of information and signals exchanged, and an explanation of the conventions used to address semiconductor memories.

2.2 BASIC MEMORY ACCESS OPERATIONS

MS11 Semiconductor Memory Systems operate in four accessing modes: read, write, optional byte handling, and pause for a write following a read. These operations are designated as follows:

a. Read Data (DATI)
b. Read data and pause (DATIP)
c. Write data (DATO)
d. Write data bytes (DATOB)

Each of these modes are briefly discussed in the following paragraphs.

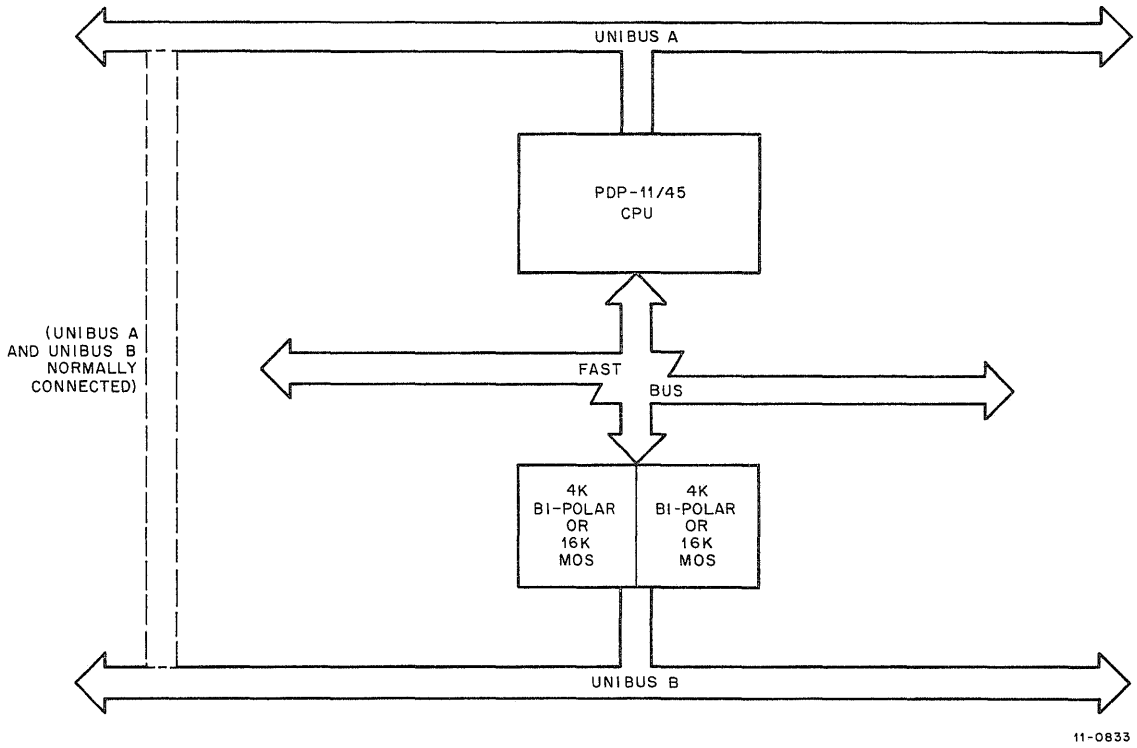


Figure 2-1 Semiconductor Memory Configuration within PDP-11/45 Systems

2.2.1 Data In (DATI) Cycle

During a DATI cycle, data in the locations addressed at the memory matrix module is loaded into the M8110 output data latch for retrieval by the initiating bus (Unibus or Fastbus). Readout of semiconductor memories is nondestructive; thus, the restore portion of the conventional core memory read cycle is not required.

2.2.2 Data In, Pause (DATIP) Cycle

The purpose of this reading mode is to hold memory secure after data is read from a set of memory addresses until that data can be revised and then written again. PDP-11 convention requires that execution of a DATIP is always followed by execution of a DATO or DATOB operation. A DATIP is a duplicate of a DATI operation except for a pause for initiation of the impending DATO or DATOB.

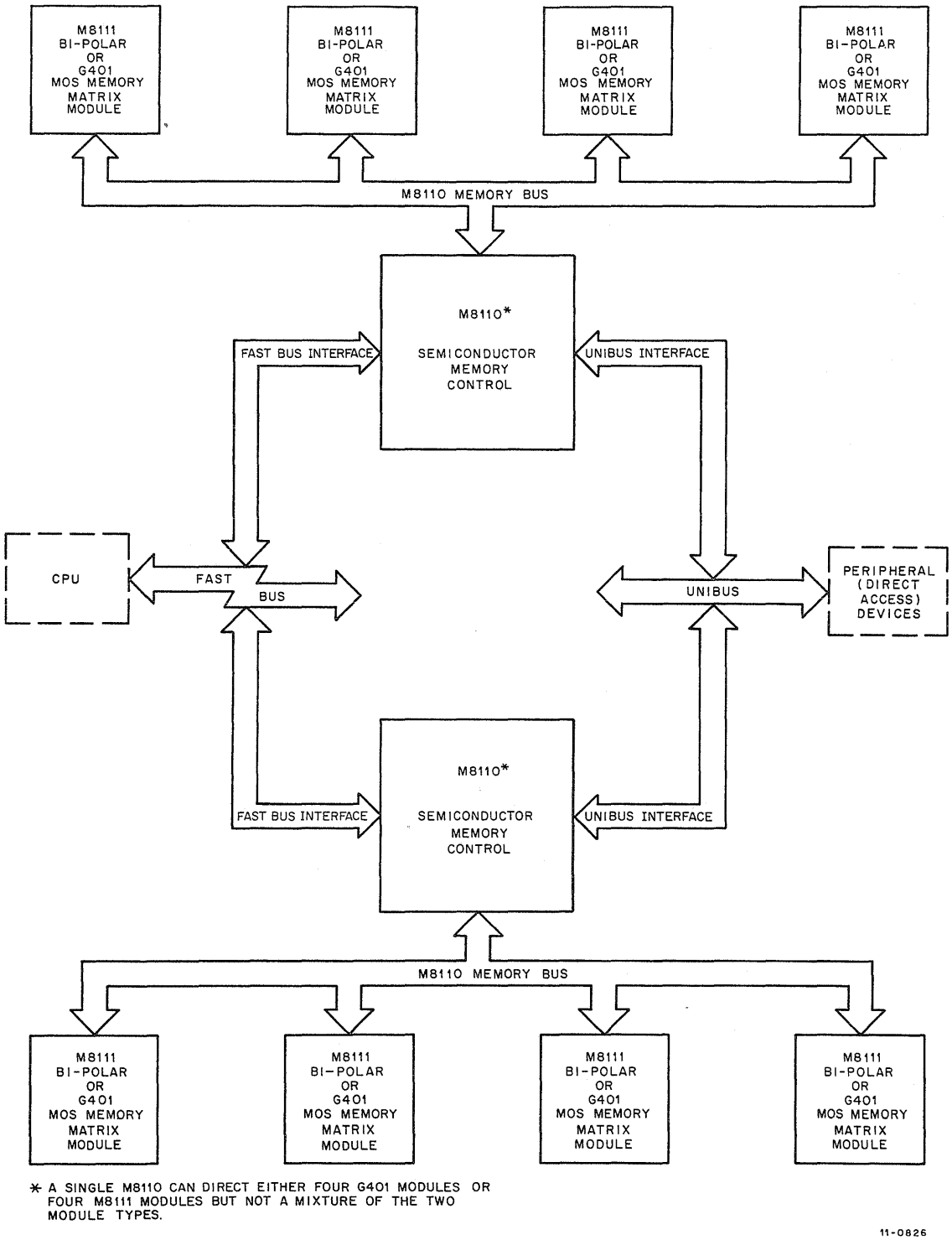


Figure 2-2 Semiconductor Memory System Interfaces

2.2.3 Data Out (DATO) Operation

A DATO, or write operation, causes data outgoing from the Unibus or Fastbus to be written one word at a time (16 bits) at the address order designated. The nature of semiconductor memories is such that locations to be written in do not require prior clearing. As a consequence, the writing of data begins immediately after cycle initiation, with no prior clearing required.

2.2.4 Data Out, Byte (DATOB) Cycle

A DATOB cycle is a duplicate of a DATO cycle, except that data is written as 8-bit bytes rather than as a 16-bit word. Decoding of each address designates whether the corresponding byte transferred from the Unibus or Fastbus is to be written as a low- or high-order byte in the 16 bits available at each memory location. Therefore, data to be written in memory as bytes must be received on the data lines corresponding to the byte position designated by the address.

2.3 FASTBUS INTERFACE

The Fastbus interface provides a high-speed, full-duplexed, dedicated data path between the processor and the M8110 Semiconductor Memory Control. The Fastbus address, data, and control lines are defined in Table 2-1.

Table 2-1

Fastbus/M8110 Interface and Control Signals

Name	Mnemonic	Source Drawing	Destination Drawing	Function
Address	DAPB BAMX ⟨05:00⟩ H SAPJ PA ⟨17:06⟩ H	DAPB SAPJ	SMCC	selects memory location
Data In	SCME MEM D ⟨15:00⟩ H	SCME	PDRA	DATI lines from Fastbus
Data Out	PDRB BR ⟨15:00⟩ B L	PDRB	SMCD	DATO lines from Fastbus
Bus Start	TMCE BUS OUT L	TMCE	SMCA	starts Fastbus-initiated memory access cycle
Memory Selected	SMCF MEM L	SMCF	TMCF	informs Fastbus that address is in semiconductor memory
Control OK	UBCA CONTROL OK H	UBCA	SMCA	informs control that current access cycle can be completed
Memory Sync	SMCA MEM SYNC (B) L	SMCA	TIGA	informs Fastbus that current memory access cycle is being completed
Control	UBCC MEM BUS C0 L	UBCC	SMCA	specifies type of memory access cycle (Table 2-2)
Control	UBCC MEM BUS C1 L	UBCC	SMCA	specifies type of memory access cycle (Table 2-2)
Bus End Clear	TMCE BEND CLR L	TMCE	SMCA	terminates current memory access cycle at M8110 control if Fastbus anticipated address is incorrect
Parity Error Halt	SMCB PE HALT L	SMCB	UBCB	initiates processor HALT on parity error
Parity Error Flag	SMCB PERF L	SCMB	UBCB	sets processor parity error flag
Parity Error Acknowledge	UBCB PERF ACKN L	UBCB	SMCB	acknowledgment by processor of receipt of parity error indication

2.3.1 Fastbus DATO Cycle

Initiation of a semiconductor memory access cycle via the Fastbus occurs when the processor places the desired memory address on the address lines (Figure 2-3). Data to be stored at this address is present on the DATO lines at the same time. The address bits are decoded in the memory selection logic and the resultant MEM signal to the processor denotes receipt of a valid address. Although the address is transmitted to both M8110 controls, only that controller having this address within its assigned range of addresses will acknowledge with the MEM signal. Processor response to MEM is TMCF FAST L, which inhibits Unibus memory addressing. TMCE BUST OUT L, also from the processor, asserts PREQ (1) H. This latter signal, together with MEM H, initiates memory timing. The memory address is now latched into the MAD register and a usable address is presented to the memory module. Required timing signals are also furnished to the memory logic. MEM BUS C0 and C1, received prior to CONTROL OK, are now decoded to indicate a DATO operation. Table 2-2 lists the four access cycle types that are decoded from these two control bits. With the subsequent CONTROL OK signal, the processor verifies the current memory access cycle. Since this is a request from the processor (PREQ), ACCESS READY LATCH H (a product of the timing operation), together with CONTROL OK, generates MEM SYNC. This latter signal performs several functions; it is returned to Fastbus to inform the processor that data is to be stored and, with MEM C1, develops DATA LATCH. The final steps are accomplished with DATA LATCH; the data to be written (Data Out) is latched into the Data In Register, placed on the bus to the memory module, and then stored at the specified location with the concurrent WRITE PULSE.

Table 2-2
Fastbus and Unibus Control Bit States

Input from Fastbus		Input from Unibus		Access Cycle to be Performed
UBCC MEM C1L	UBCC MEM C0L	BUSB C1 L	BUSB C0 L	
Usable Signal		Usable Signal		
SMCA MEM C1L	SMCA MEM C0L	SMCH UBC1 H, L	SMCH UBC0 H, L	
0	0	0	0	DATI
0	1	0	1	DATIP
1	0	1	0	DATO
1	1	1	1	DATOB

The KB11 Processor, during execution of a current instruction, attempts to predict the address of the word needed next for purposes of increased operating efficiency. After each instruction fetch, the processor initiates another bus cycle to fetch the word following the current instruction cycle. If the instruction currently being executed requires data, not from the next word, but from a different address, then the processor terminates that bus cycle aimed at retrieving the next word. This terminating process results in the processor issuing TMCE BEN CLR L to the semiconductor memory control. At the control that previously acknowledged the address associated with the discontinued bus cycle by responding with SMCF MEM L, TMCE BEND CLR L terminates the memory access cycle initiated by TMCE BUST OUT L.

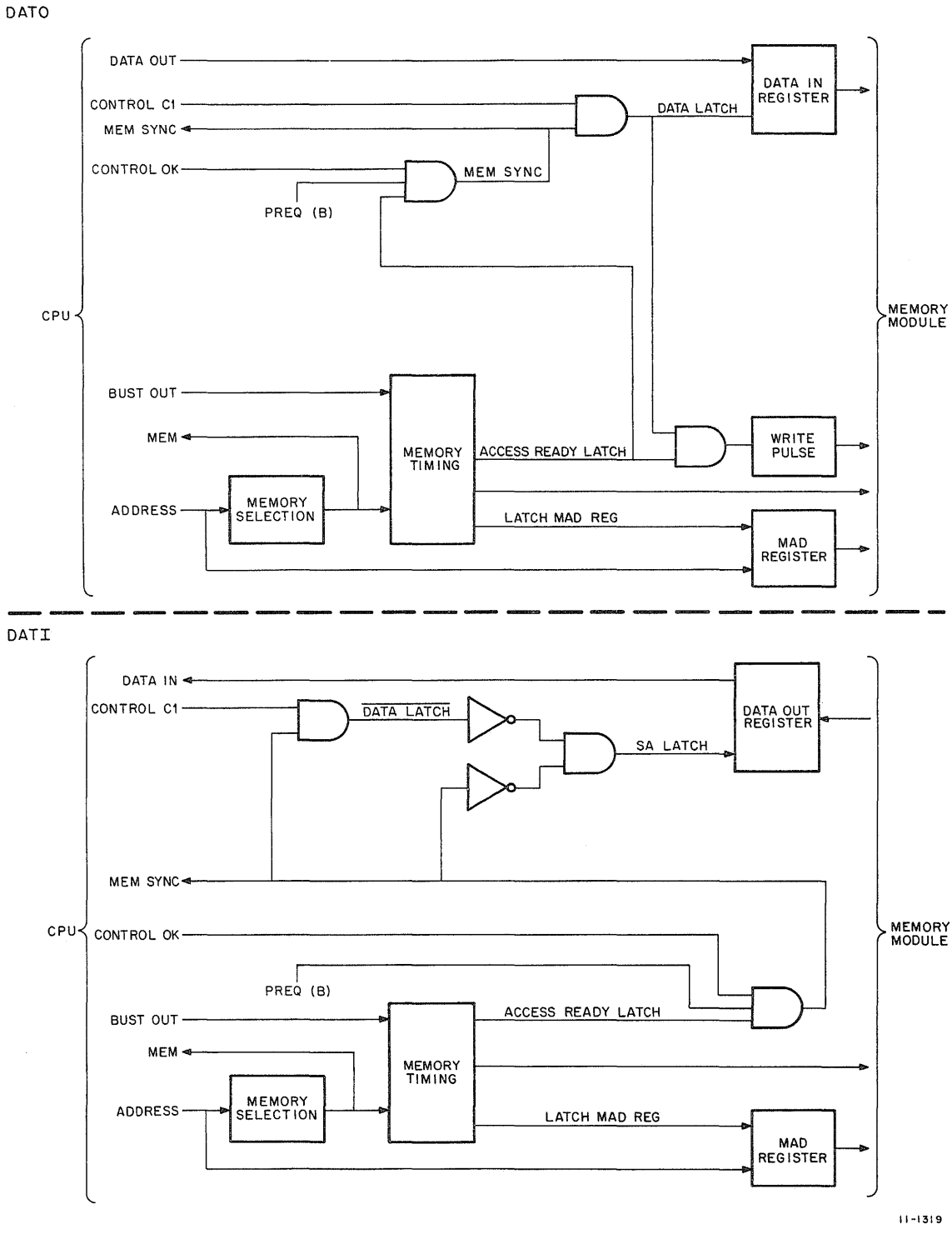


Figure 2-3 Fastbus Interface

2.3.2 Fastbus DATI Cycle

If the Fastbus-initiated access cycle is a DATI or DATIP (Figure 2-3), the sequence is essentially the same as when DATO was executed. When the memory address from the Fastbus is decoded, MEM is returned to the processor. The BUST OUT signal from the processor that follows asserts PREQ (1) H. This latter signal, together with MEM H, initiates memory timing, the memory address is placed on the lines to the memory module. After CONTROL OK is received, the timing sequence continues without further processor interruption. ACCESS READY LATCH, a product of the timing process, generates the MEM SYNC signal. Unlike the DATO operation, MEM BUS C1 (Table 2-2) is a 0 for DATI and DATA LATCH is inhibited. However, due to the signal levels used, SA LATCH is set at the termination of the MEM SYNC pulse. The data from the desired address in the memory matrix is then transmitted, as DATA IN, from the Data Out Register via Fastbus to the processor.

Although the two M8110 parity diagnostic registers are addressed and loaded through the Unibus interface, parity error indicators PE HALT and PERF are relayed to the processor through the Fastbus. The receipt of either indicator causes the processor to issue PARITY ERROR ACK to the pertinent M8110 control.

2.4 UNIBUS INTERFACE

Data transfers through the Unibus between the semiconductor memory system and the processor (or other devices) are conducted on a master/slave basis with the memory in all circumstances having slave status (refer to the *PDP-11 Unibus Interface Manual*). Unlike the Fastbus interface, data lines between the Unibus and the M8110 con control are bidirectional. The information and control signals passed between the Unibus and the M8110 Semiconductor Memory Control module are defined in Table 2-3.

Table 2-3
Unibus/M8110 Interface Information and Control Signals

Name	Mnemonic	Source	Destination	Function
Address	BUSB A ⟨17:00⟩ L	BUSB	SMCH	selects memory location
Data	BUSB D ⟨15:00⟩ L	BUSB	SMCH	provides for bidirectional data transfer between Unibus and semiconductor memory
Master SYNC	BUSB MSYNC L	BUSB	SMCH	initiates memory access cycle specified by state of UBCC C0 and C1
Slave SYNC	BUSB SSYNC L	SMCF	BUSB	acknowledges connection
Control	BUSB C0 L	BUSB	SMCH	specifies type of memory access cycle (Table 2-2)
Control	BUSB C1 L	BUSB	SMCH	specifies type of memory access cycle (Table 2-2)
dc Power Low (Bus A)	BUSA DCLO L	BUSA power control modules	SMCH	indicates dc voltage out of tolerance on bus A
dc Power Low (Bus B)	BUSB DCLO L	BUSB power control modules	SMCH	indicates dc voltage out of tolerance on bus B

At the M8110, all information and control-signal interchange with the Unibus is routed through the SMCH logic on the M8110 control. This logic consists of a drive/receiver interface designed for high-speed information and control-signal transmission and receipt from remote locations over the Unibus cable module.

2.4.1 Unibus DATO Cycle

A memory access cycle is initiated (Figure 2-4) from the Unibus when the processor or direct access device places the memory address on the input lines to both M8110 controls. Only that control where the address falls within the established address range will have its memory selection logic activated. Control bits C0 and C1 are also present at the control input at this time; they are decoded (Table 2-2) to determine the type of memory access cycle to be executed. The data to be stored is concurrently available on the DATA lines. Enabling of the address decoding circuitry occurs with the arrival of MSYNC from the Unibus. The subsequent BREQ initiates the memory timing sequence. One of the first signals generated, BREQ IN PROG, provides a required condition for DATA LATCH. Latching of the memory address into the MAD Register occurs next; the memory matrix module is thereby presented with a usable storage address prior to the data being strobed over the memory bus. Following a delay, ACCESS READY LATCH simultaneously produces DATA LATCH and MEM SSYNC. The latter signal is returned, via the Unibus, as BUSB SSYNC, informing the processor that the selected control has accepted and stored the data. DATA LATCH results in the DATA being gated into the Data In Register and then placed on the bus to the memory matrix. Concurrent with this, DATA LATCH produces the WRITE PULSE, the function of which is to store the data at the prescribed memory location. The advent of SSYNC disables MSYNC and the access cycle is complete with respect to the Unibus and M8110 interfacing.

2.4.2 Unibus DATI Cycle

A DATI memory access operation (Figure 2-4) is similar to the Unibus DATO procedure described above. The access cycle is initiated in the M8110 logic on receipt of the memory address. Control bits C0 and C1 are input at the same time; C1 is a 0. However, unlike DATO, DATA is not sent from the processor in a DATI operation; the bidirectional data lines will be used to carry the data retrieved from memory back to the processor. MSYNC results in BREQ, which triggers the timing sequence that follows. BREQ IN PROG fulfills the second requirement for MEM SSYNC and the memory address is latched into the MAD register. The selected memory address is then delivered to the memory matrix along with required timing signals. MEM SSYNC is brought up, after a delay, by ACCESS READY LATCH. MEM SSYNC notifies the processor that the timing sequence is completed and that the data requested is available for acceptance. Although SA LATCH is set, the read data bypasses the Data Out Register en route to the Unibus.

2.5 MEMORY BUS

Figure 2-5 is a simplified block diagram of the semiconductor memory bus. This bus is part of the M8110 Semiconductor Memory Control module and implements the multiplexing of DATO and DATI operations between the Fastbus, Unibus, and semiconductor memory system storage.

The multiplexing of memory access operations over the memory bus is governed by priority arbitration logic on the M8110 control. This logic arbitrates memory access requests only when simultaneous requests are received from the Unibus and Fastbus. In such arbitration, Unibus memory access cycles have higher priority. In all other cases, memory is multiplexed between the Fastbus and the Unibus on a "first come, first served" basis. In addition, any memory access cycle, once started, locks out all other bus requests until completed. The DATI side of the M8110 memory bus is coupled to both the Fastbus data-in lines and the Unibus interface so that disposition of data on this portion of the memory bus is handled by the requesting bus.

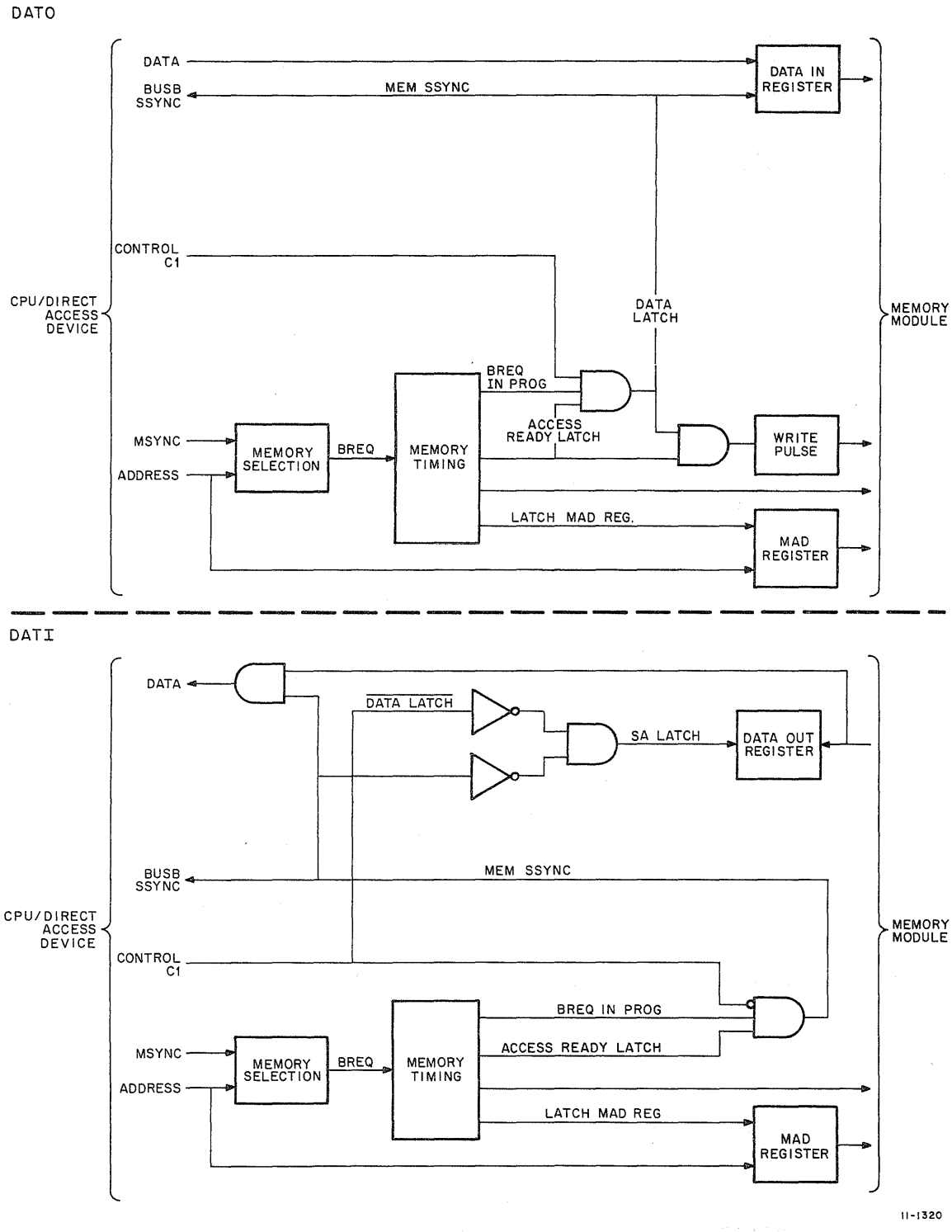


Figure 2-4 Unibus Interface

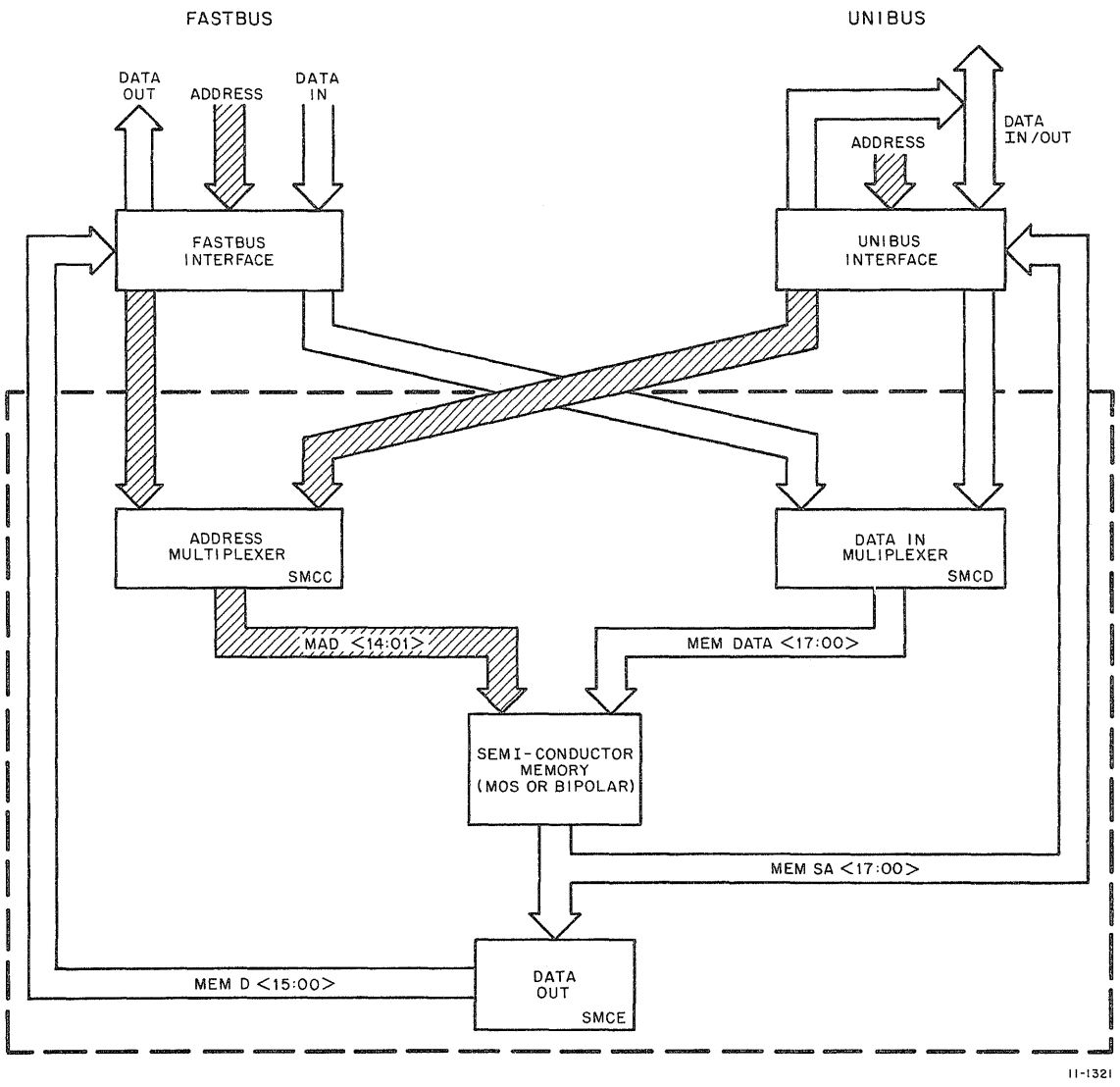


Figure 2-5 Semiconductor Memory Bus, Simplified Block Diagram

2.6 SEMICONDUCTOR MEMORY ADDRESSING

The M8110 Semiconductor Memory Control module, whether directing bipolar or MOS memories, always processes an incoming Fastbus or Unibus address in the same manner. This process involves two simultaneous actions by each M8110 control: address examination and address mapping. In order to clarify the effects of these actions, the specific description of each action is preceded by a brief description of the PDP-11 addressing scheme.

In the PDP-11 System, a 16-bit word is addressed by an even binary number. The high-order byte in that word is addressed by the next higher number in the binary address count, which is an odd number. In this manner, the state of the least-significant bit in an address (bit 0) determines whether a full word (or low-order byte) or the high-order byte is being addressed. Consequently, the address for a 16-word (or the low order byte in any word) is always even, and the address for a high-order byte in any word is always odd.

For example:

Typical address for a full 16-bit word or low-order byte	173346_8
Address for the high-order byte in the same word	173347_8

2.6.1 Address Decoding at the M8110 Control

Figure 2-6 shows how each M8110 control examines Unibus and Fastbus addresses. At each control, the states of address bit ⟨17:13⟩ are compared with equivalent jumper-wired states to decode the address. Address bits ⟨17:16⟩ designate up to 32K of semiconductor memory locations out of a total memory capacity of 128K. Decoding of address bit 15 designates the specific M8110 control being addressed. Therefore, that control whose jumper-wired states of bits ⟨17:15⟩ match the states of address bits ⟨17:15⟩ has the location being addressed within its total range of memory locations. Decoding address bits ⟨14:13⟩, as compared with jumpered states at each module, designate that the memory location specified by the address being examined is within one of the 4K-word pages comprising the semiconductor memory. When all conditions of address decoding, as specified by jumper connections at either control, are satisfied, then mapping of that address is enabled at the selected control.

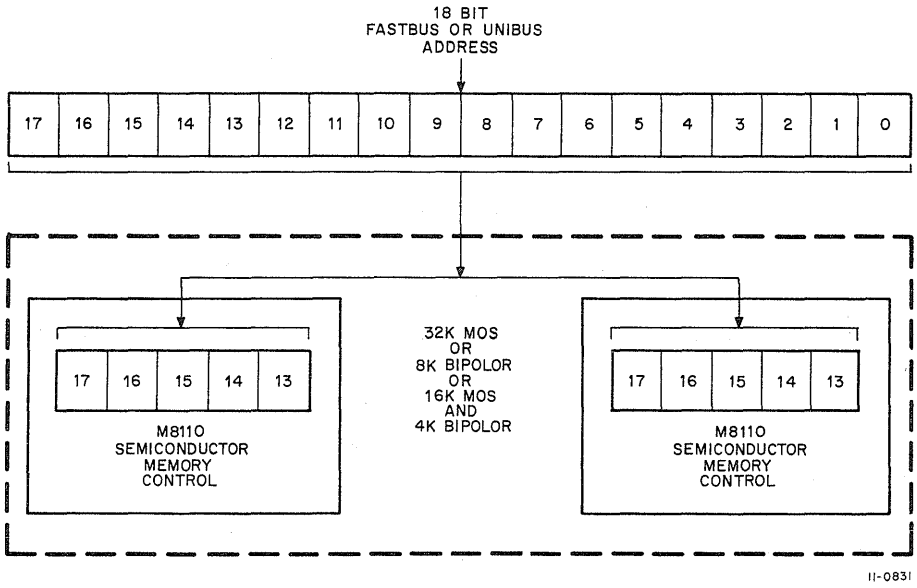
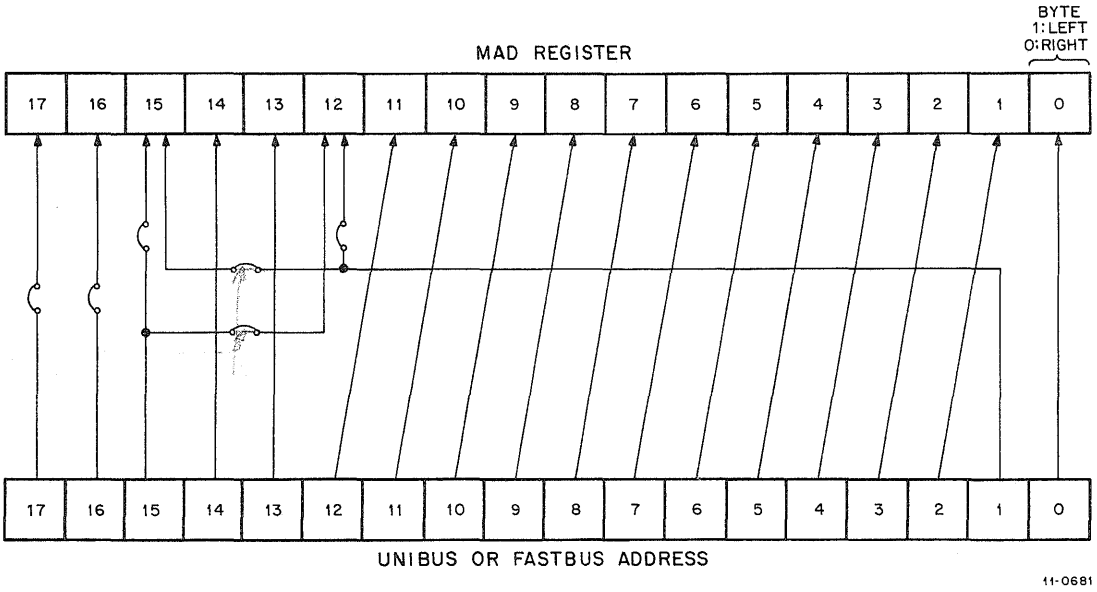


Figure 2-6 Semiconductor Memory Address Examination

2.6.2 Address Mapping at the M8110 Control

The manner in which addresses are examined by the M8110 requires that each incoming Fastbus or Unibus address must be mapped into the MAD register. This mapping action, as illustrated in Figure 2-7, amounts to the shifting of address bits ⟨12:02⟩ one position to the right, and the routing of address bits 01 and 15 according to specific jumper configurations. The installation of required address jumpers is described in detail in Paragraph 3.4.1.



NO LONGER THERE

Figure 2-7 Semiconductor Memory Address Mapping

2.6.3 MOS Memory Matrix Module Address Decoding

The MAD ⟨14:13⟩ and ⟨02:01⟩ bits are decoded at each G401 MOS Memory Matrix module when the directing M8110 control is addressed (Figure 2-8). Because the states of MAD ⟨14:13⟩ are compared to jumpered states unique to each module, the module with matching states is the module to be accessed. This equality at the addressed G401 module, in turn, enables examination of MAD ⟨02:01⟩. The states of these bits are decoded at a logic structure on the G401 module to determine which of the four 1024 X 16-bit word block contains the location being addressed. Output from this structure enables addressing of the pertinent 1024-word blocks and implements access to the address location.

2.6.4 Bipolar Memory Matrix Module Address Decoding

MAD bits ⟨14:10⟩ are decoded on the M8110 control to determine which 1K segment of the possible 16K addresses is being addressed (Figure 2-9). MAD bits ⟨09:08⟩ are decoded to select which 256-word section of the 1K matrix module is being addressed. MAD bit 12 and MAD bits ⟨07:01⟩ select the particular word within each 256-word section that is being addressed.

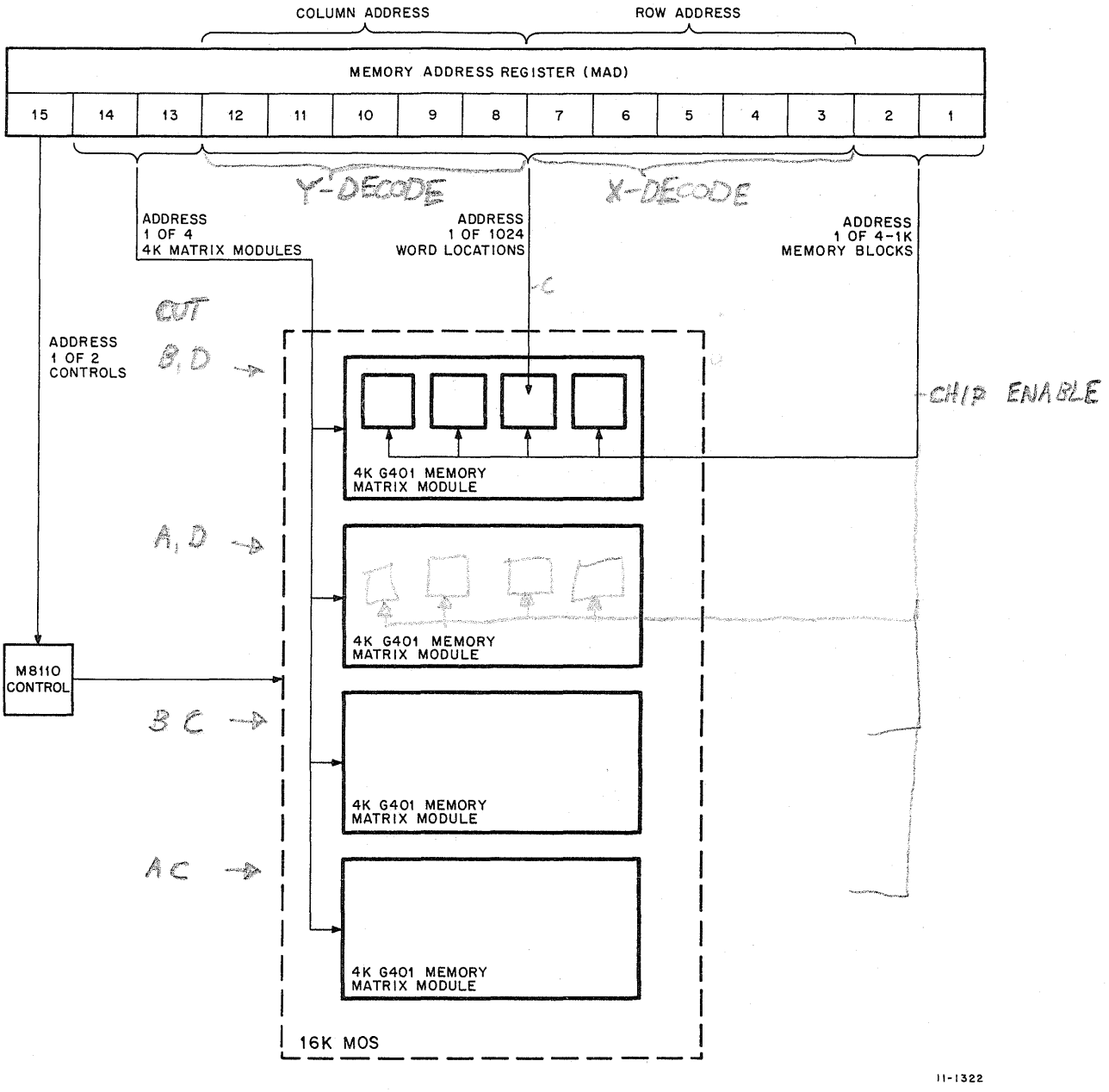


Figure 2-8 MOS Memory Matrix Address Examination

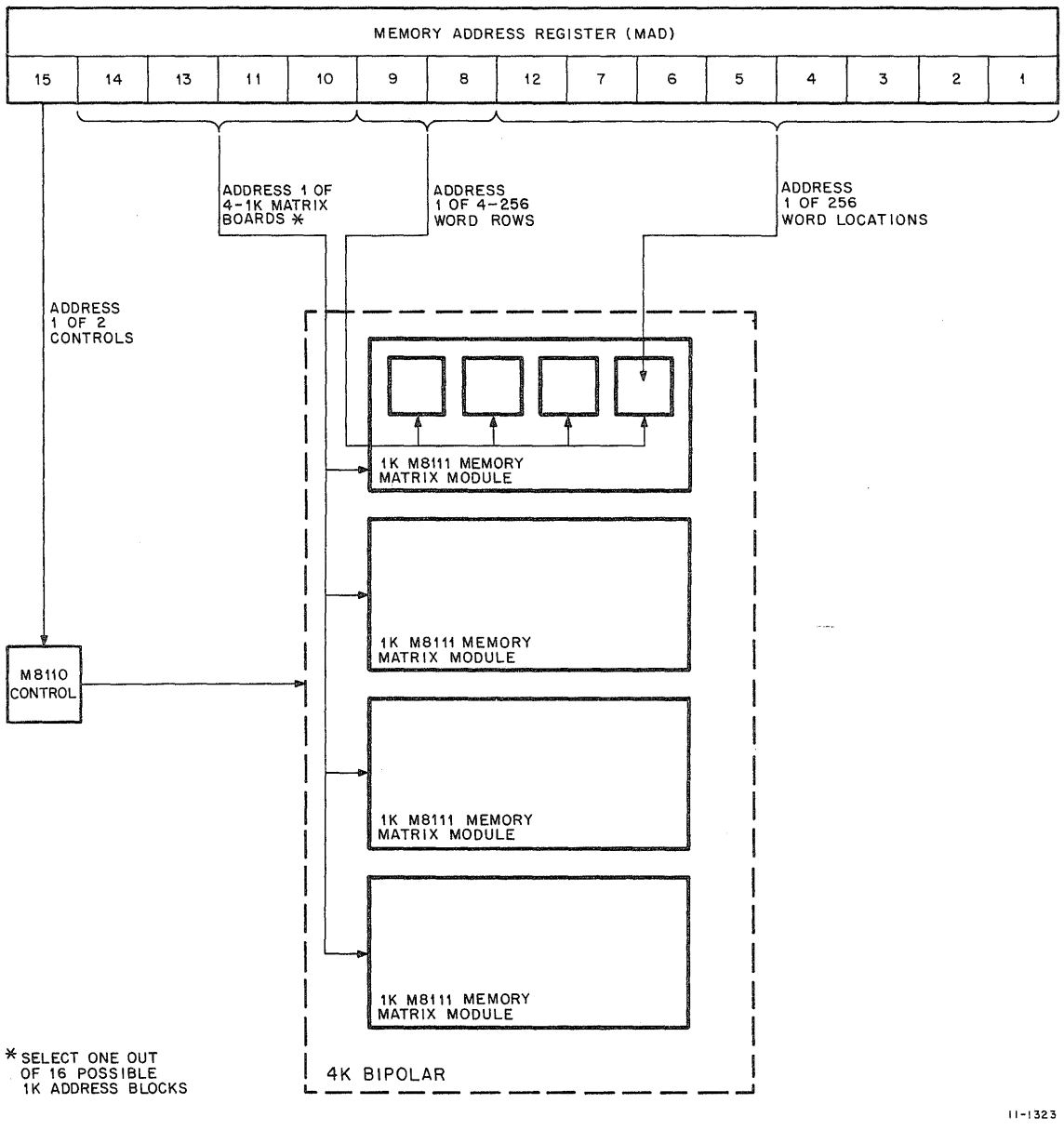


Figure 2-9 Bipolar Memory Matrix Addressing

CHAPTER 3
LOGIC DESCRIPTION

3.1 INTRODUCTION

As described in Paragraph 1.1, an MS11 Semiconductor Memory System can take two forms: bipolar and MOS. Both forms of semiconductor memory use the M8110 Semiconductor Memory Control module. The descriptions of semiconductor memory system logic follow this system structure, starting with the G401 MOS Memory Matrix module and the M8111 Bipolar Memory Matrix module; followed by descriptions of the M8110 control selection, memory bus, and interface logic. These logic descriptions are then interrelated through a detailed description of semiconductor memory control operation, including all memory access cycles and the diagnostic parity function. Finally the refresh logic, which pertains only to the MOS semiconductor memory system, is described in detail.

3.2 G401 MOS MEMORY MATRIX MODULE LOGIC

The memory capacity of the G401 is formed by seventy-two 1103-type fully decoded, random-access, 1024 X 1-bit dynamic memory circuits. These 4096-word memories are directly addressed on the basis of 1024 18-bit words (Figure 3-1). The specific set of 1024 words addressed is determined by the states of MAD register bits 01 and 02. The states of these bits, asserted as MAD 01 (1) H and MAD 02 (1) H on drawing MOSA, are decoded to enable the control levels CENABLE and PRECHARGE to the specific set of 1024 words to be addressed for a DATO or DATI. The result of MAD 01 (1) H and MAD 02 (1) H decoding is a set of gating control levels designated MOSA A H, MOSA B H, MOSA C H, and MOSA D H.

Decoding of MAD 01 (1) H and MAD 02 (1) H is performed by the logic shown on drawing MOSA. This logic is enabled by the states of address bits MAD 13 and MAD 14, that specify which of the four G401 MOS memory modules directed by a given control (Figure 2-8) is being addressed. The states of MAD 13 and MAD 14 are uniquely jumper-connected at each G401 module to condition the gating of control levels MOSA A H, B H, C H, and D H only at the memory module addressed. The states of MAD ⟨14:13⟩, as jumpered, also assert levels MOSA SEL 13 H and MOSA SEL 14 H to enable the G401 read amplifiers at the addressed memory module in case the current access cycle is a DATI.

Table 3-1 lists the required jumper configuration for the assignment of the associated 4K block of MOS memory addresses, while Table 3-2 indicates the control levels generated, and the 1K memory block selected, from MAD 01 and MAD 02. Control levels MOSA A, MOSA B, MOSA C, and MOSA D gate SMCA PRECHARGE, SMCA CENABLE, and WRITE PULSE HIGH/LOW to access one of four sets of 1024 words. For example, if a G401 MOS matrix has jumpers C and B installed, then that matrix contains memory locations XX4096 through XX8191. (Since there are $131,072_{(10)}$ possible addresses, XX equals 00 to 13. As described in Paragraph 3.4.1, Fastbus/Unibus address decoder bits ⟨17:15⟩ determine these higher range address assignments.) Any address, directed to this memory module, where MAD 14 is a 0 and MAD 13 is a 1 will cause the matrix to recognize and respond to

the address. Further definition of the same address is made by the MAD 01 and MAD 02 configuration. If MAD 02 is a 1 and MAD 01 is a 0, then control levels MOSA D and MOSA A are generated. As indicated by Table 3-2, these two control levels will select the third 1K memory segment, in this case locations XX6144 through XX7167.

Table 3-1
MOS Matrix Selected Address Configuration (4 of 16K)

MAD		REQUIRED JUMPERS		MOS Matrix Memory
14	13	(MAD 14)	(MAD 13)	Address Assignment
0	0	C	A	0–4095
0	1	C	B	4096–8191
1	0	D	A	8192–12,287
1	1	D	B	12,288–16,383

Table 3-2
MOS Matrix Control Level Generation and Selected Memory
Address Block (1 of 4K)

MAD		CONTROL LEVELS GENERATED			Memory Address
02	01	(MAD 02)		(MAD 01)	Block Selected
0	0	MOSA B	•	MOSA A	0–1023
0	1	MOSA B	•	MOSA C	1024–2047
1	0	MOSA D	•	MOSA A	2048–3071
1	1	MOSA D	•	MOSA C	3072–4095

3.2.1 MOS Memory Writing

Address lines MAD ⟨12:03⟩ (drawings MOSA through MOSJ) are input to the MOS memory module and enable a level-shifting NAND gate structure formed by 3-input level shifters (E1 through E5). Outputs are the MOS levels +1V and +19V, so that a +3V TTL input is level-shifted to +1V, and TTL ground input is level-shifted to +19V. Each gate output is propagated through a series-damping resistor to the corresponding 1103 type MOS memory circuit address input terminal. The access control levels PRECHARGE, CENABLE, WRITE PULSE HIGH, and/or WRITE PULSE LOW are also input to this level-shifting NAND gate structure (E13, E14, E39, E40, E65, E66, E91, and E92) and are propagated to the corresponding 1103 input terminals in the same manner. The use of damping resistors at the gate output effectively eliminates any potential ringing problems.

As shown on drawings MOSA through MOSJ, the level-shifting NAND gate structure is configured to form two duplicate level-shifting gate structures: one to access the low-order byte and one to access the high-order byte. The only logical difference in these duplicate structures is that WRITE PULSE LOW H conditions the structure accessing the low-order byte, and WRITE PULSE HIGH H conditions the structure accessing the high-order byte. The outputs from each gate structure connect in parallel to the address and control terminals for the 36 circuits storing the four groups of 1024 bytes. With these gating structures conditioned by the appropriate access control levels, the state of gating control levels MOSA A H, MOSA B H, MOSA C H, and MOSA D H (Table 3-2) enable accessing the specific 1024 bytes or words designated by the current address.

The access levels CENABLE L, PRECHARGE L, WRITE PULSE LOW L, and WRITE PULSE HIGH L are inverted and buffered by two buffer gates (MOSC, E9 and E10) to provide the drive necessary to access the MOS memory.

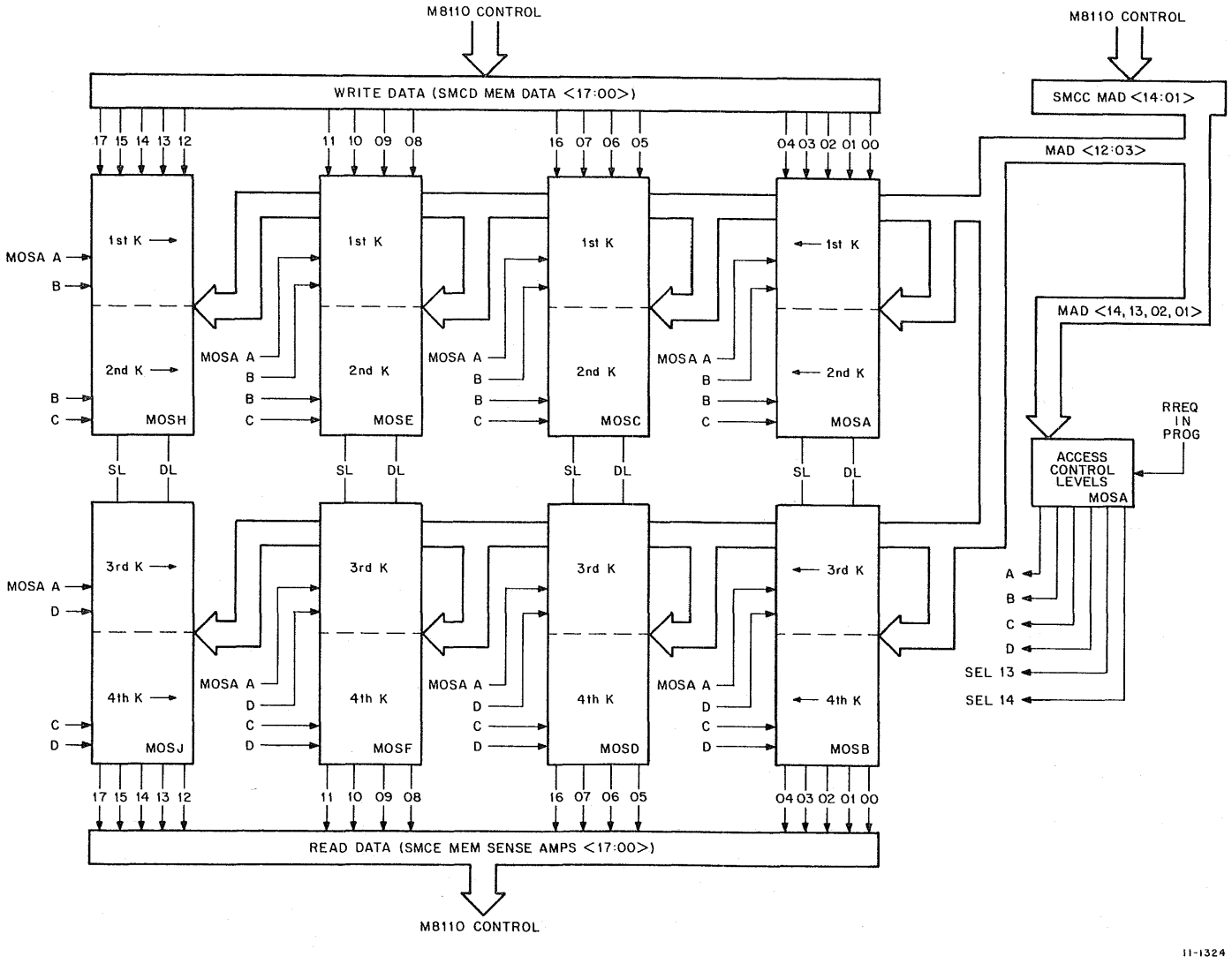


Figure 3-1 MOS Memory Matrix, Block Diagram

3.2.2 MOS Memory Reading

At the selected G401 MOS memory module, the states of MAD bits 13 and 14 will assert MOSA SEL 13 H and MOSA SEL 14 H from gates E6. These levels enable a parallel sense-amplifier network made up of 18 sense amplifiers, one for each memory bit. Each sense amplifier consists of one element of a 75108 dual-line receiver with open collector output. The input to each sense amplifier is wire-ORed to the output of four memory circuits. As a result, the input to each sense amplifier is the wire-OR of 1024 memory bit locations. Therefore, when a given word is addressed, the content of the addressed location is input to the sense amplifiers. Note that the second input to each sense amplifier is an unterminated line paralleling the first input. The purpose of this line is to cancel common-mode noise generation on the adjacent sense line. The DATA output from each 1103 memory circuit functions as an active current source so that output is 900 μA for logic 1 and 0 μA for logic 0. In addition, the sensed output from each sense amplifier is a TTL output; therefore, output logic levels are 3V = 1 and 0V = 0.

In summary, during a given DATI cycle, as the location to be retrieved is addressed, the data stored in that location is placed on the internal lines MEM SA ⟨17:00⟩ to the output data multiplexing logic shown on drawing SMCE.

3.3 M8111 BIPOLAR MEMORY MATRIX MODULE LOGIC

The maximum storage capability of an M8111YA Bipolar Memory Matrix module is formed by 72 fully decoded, random-access, 256-bit bipolar TTL memory integrated circuits, all interconnected to form a 1024-word X 18-bit memory (Figure 3-2). Each memory chip is organized as 256 1-bit words. Therefore, eighteen ICs comprise a 256 X 18-bit memory, and four rows of 256 X 18 bits provide the 1K capacity.

The M8111 Bipolar Memory Matrix module is identical to the M8111YA in every respect, except that the memory word is 16 bits without byte parity. Therefore, the maximum memory capacity of an M8111 is formed by 64 memory circuits.

The module logic functionally divides into two sections, as shown in the drawings for the matrix control BIPA and BIPB, and the memory matrix proper, BIPC, BIPD, BIPE, BIPF, BIPH, BIPJ, BIPK, and BIPL. The description of the detailed logic which follows is based on this functional division; it is applicable to both the M8111 and M8111YA modules.

3.3.1 Memory Matrix Control

The BIPA and BIPB matrix control logic performs five basic functions with respect to the memory matrix portion of an M8111 module. First, address lines from the M8110 control are buffered to provide the fanout necessary to address the bipolar memory circuits. Second, DATA lines from the M8110 control are inverted providing the proper logic level polarity to the memory matrix, with accompanying write pulses being buffered for necessary fanout. Third, address bits MAD ⟨14:13⟩ and ⟨11:10⟩ (equivalent to Fastbus or Unibus address bits ⟨14:11⟩) are decoded to enable the specific 1024-word matrix out of the four 1024-word bipolar modules directed by the M8110 control (Figure 2-9). Fourth, CENABLE from the M8110 is buffered to provide required fanout. Fifth, MAD ⟨09:08⟩ are decoded to enable the 256-word section at the selected module containing the addressed location.

3.3.1.1 Address Buffer – The M8111 address buffer (drawing BIPA) is an 8-stage parallel buffer which expands each of the eight address lines MAD ⟨07:01⟩ and MAD 12 into four separate lines per bit, thereby providing necessary fanout to the matrix. For each address line input to the buffer from the M8110 control, four lines are output to the memory matrix, one line for each 256-word section of a 1024-word bipolar memory module. Each stage consists of an input inversion stage (one element of a 74S04 hex inverter) and two 74S40 dual 4-input

buffer NAND gates. All four buffer gates in each buffer stage are conditioned at three inputs by a common line to +3V (drawing BIPA). The enabling input to the buffer is the inverted address so that the polarity of the expanded output address matches that of the input address. The expanded addresses connect to a corresponding 256-word section of M8111 bipolar memory as shown in Table 3-3.

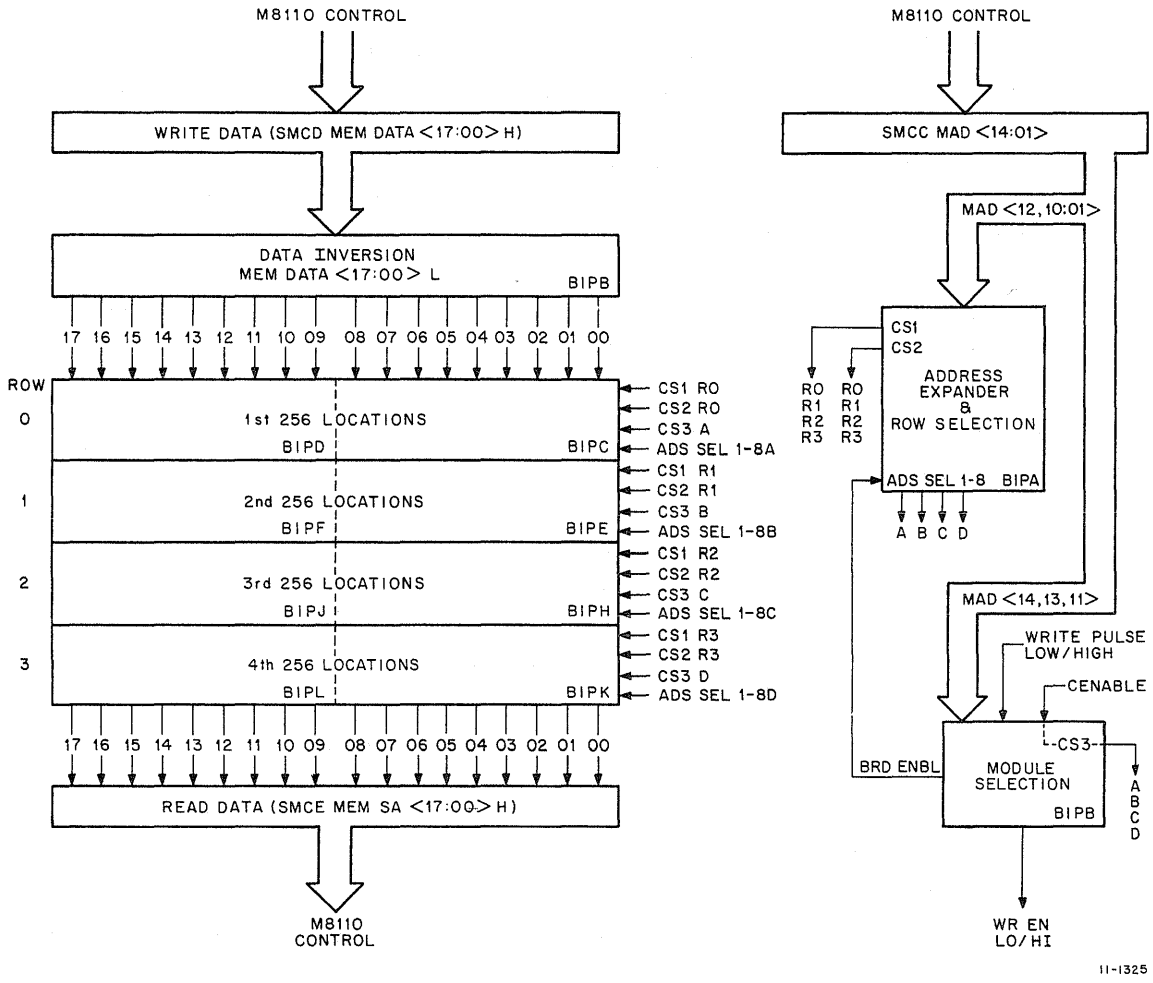


Figure 3-2 Bipolar Memory Matrix

Table 3-3
Expanded M8111 Memory Address Allocation

Expanded Addresses	Memory Area Addressed
BIPA ADRS SEL ⟨8A:1A⟩	0 to 255_{10}
BIPA ADRS SEL ⟨8B:1B⟩	256 to 511_{10}
BIPA ADRS SEL ⟨8C:1C⟩	512 to 767_{10}
BIPA ADRS SEL ⟨8D:1D⟩	768 to 1023_{10}

3.3.1.2 **Data Inversion and Write Pulse Fanout Logic** – Input to the data inversion logic are the DATA lines from the M8110 control SMCD MEM DATA ⟨17:00⟩ H (drawing BIPB). This 18-stage inversion logic, formed by four 74S04 hex inverters, drives inverted data lines to the bipolar memory matrix. Note that DATI lines from the M8111 bipolar module to the M8110 controls are propagated directly from each memory circuit on MEM SA ⟨17:00⟩ H, that is, the data output from the four 256-word sections are wired-ORed to the M8110 control.

The two write-enabling pulses that can be asserted at the M8111 module (BIPB) during a DATO are SMCA WRITE PULSE LOW L and WRITE PULSE HIGH L, which enable writing of low-order and/or high-order bytes, respectively, in the addressed location. If a full 16-bit word is being written, both levels will be asserted simultaneously. Each write pulse is buffered in parallel by two identical buffer networks to provide the necessary fanout capability. For example, SMCA WRITE PULSE LOW L, when asserted, is first inverted by one stage of a 74S04 hex inverter. Inverter output then enables both gates of a 74S40 NAND buffer (E13). With SMCA WRITE PULSE LOW L asserted, buffer gate outputs are BIPB WR EN LO A L and BIPB WR EN LO B L. When WRITE PULSE HIGH L is asserted, BIPB WR EN HI A L and BIPB WR EN HI B L are asserted. BIPB WR EN LO A and BIPB WR EN LO B enable writing a low-order byte and BIPB WR EN HI A and BIPB WR EN HI B enable writing a high-order byte. When all four pulses are asserted simultaneously, writing a full word at the addressed location is enabled.

3.3.1.3 **Address Examination Logic** – The M8111 Bipolar Memory Matrix module decodes Unibus or Fastbus address bits ⟨14:11⟩ (drawing BIPB). The relationship of address bits to MAD register bits is shown in Table 3-4.

Table 3-4
Address Bit to MAD Bit Translation

Fastbus or Unibus Address Bit	MAD Register Bit
ADR 14	MAD 14
ADR 13	MAD 13
ADR 12	MAD 11
ADR 11	MAD 10
ADR 10	MAD 09
ADR 09	MAD 08

MAD register bits 14 and 13 in both states, along with MAD 11 (1) H, are jumpered at BIPB for input to a triple 3-input NAND gate, E8. Unibus or Fastbus address bits ⟨14:11⟩ serve to place a given address within a 16K set of addresses. Therefore, the selective jumpering of these address bit inputs at an M8111 memory module can designate that memory module as having a unique 1K set of consecutive addresses within the total set of 16K addresses. Table 3-5 lists jumper connections and the corresponding address set selected by each connection configuration, along with the (MAD) address bit configuration necessary to access the module. For example, if jumpers D, E, J, and A are installed, the memory module is assigned addresses XX7168 through XX8191. Then a Fastbus or Unibus address within this range (MAD 14 = 0, MAD 13 = 1, MAD 11 = 1, and MAD 10 = 1) will cause this memory module to respond.

Fastbus or Unibus address bits ⟨10:09⟩ are translated by the M8110 control, as shown in Table 3-4, as MAD ⟨09:08⟩. The states of these address bits designate which 256-word section of the 1024-word matrix contains the location being addressed. These bits are received at each M8111 module and inverter-buffered by two parallel, dual-stage inverter networks to assert the corresponding levels BIPA A 09 L, BIPA A 09 H, BIPA A 10 L, and BIPA A 10 H. These levels are then input to an 8-stage logic network formed by four dual power gate units: E6, E7, E14, and E15. This network is conditioned by the four state combinations of BIPA ⟨A10:A09⟩ and +3V. The network is

enabled when the level BIPB BRD ENBL and the appropriate state of MAD 10 are asserted as a consequence of address decoding. Enabled output from this network consists of one of four pairs of enabling levels being true, as listed in Table 3-6, to enable the 256-word section of bipolar memory being addressed. These enabling levels are low when asserted and constitute two of the three required chip-select inputs. The third chip-select input is generated by SMCA CENABLE L from the M8110 control. This signal is received by E9 on BIPB that drives four gates (E4 and E5) in parallel to provide the required fanout. The outputs are BIPB CS3 ⟨A, B, C, D⟩ L. Each output drives one row of memory chips.

Table 3-5
Bipolar Matrix Selected Address Configuration (1 of 16K)

MAD				Required Jumpers				Memory Address Assignment
14	13	11	10	(MAD 14)	(MAD 13)	(MAD 11)	(MAD 10)	
0	0	0	0	D	F	H	B	0 to 1023
0	0	0	1	D	F	H	A	1024 to 2047
0	0	1	0	D	F	J	B	2048 to 3071
0	0	1	1	D	F	J	A	3072 to 4095
0	1	0	0	D	E	H	B	4096 to 5119
0	1	0	1	D	E	H	A	5120 to 6143
0	1	1	0	D	E	J	B	6144 to 7167
0	1	1	1	D	E	J	A	7168 to 8191
1	0	0	0	C	F	H	B	8192 to 9215
1	0	0	1	C	F	H	A	9216 to 10,239
1	0	1	0	C	F	J	B	10,240 to 11,263
1	0	1	1	C	F	J	A	11,264 to 12,287
1	1	0	0	C	E	H	B	12,288 to 13,311
1	1	0	1	C	E	H	A	13,312 to 14,335
1	1	1	0	C	E	J	B	14,336 to 15,359
1	1	1	1	C	E	J	A	15,360 to 16,383

Using the example given above, further definition of the memory location within the 1K memory block (addresses XX7168 through XX8191) is effected using the states of MAD 08 and MAD 09. If MAD 08 = 1 and MAD 09 = 0, then the respective BIPA A09 and BIPA A10 signals generate BIPA CS1 R1L and BIPA CS2 R1L. These signals, together with CENABLE generated BIPB CS3 BL, will address the second 256 group of locations within the 1K block, i.e., locations XX7424 through XX7679. MAD 12 ⟨7:1⟩ (BIPA ADRS SEL ⟨8:1⟩) select the discrete location from this 256 location group.

3.3.2 Bipolar Matrix

The 1024-word bipolar storage matrix contained on the M8111 memory module is organized as four rows with 256 words in each row. If the module is equipped for parity, each of these four rows is made up of 256 18-bit words. If the module is not equipped for parity, each row is made up of 16-bit words. A bipolar matrix with parity is formed by 72 memory circuits; a non-parity matrix is formed by 64 memory circuits. Each of the circuits in a given 256-word row is enabled by a unique set of enabling levels as shown in Table 3-6, in coincidence with BIPB BRD ENBL H. In addition to the 256 X 1-word storage capacity, each memory circuit contains integral write and sense amplifiers so that data is written directly into, or read directly from, each circuit in the matrix as addressed. If the current memory access cycle is a DATO, the M8110 control would, following assertion of SMCA CENABLE L, assert one or both of the pulses SMCA WRITE PULSE LOW L and SMCA WRITE PULSE

HIGH L, depending upon whether a byte or a full word is being written. At this point in DATO, the specific memory location is addressed, and the data to be written is present so that assertion of WR EN LO A L/WR EN LO B L, and/or WR EN HI A L/WR EN HI B L will enable the write amplifiers on the memory circuits addressed.

Table 3-6
Address Decoding for Memory Circuit Enabling

BIPA A10 (MAD 09)	BIPA A09 (MAD 08)	Enabling Levels	Memory Locations Selected
0	0	BIPA CS1 R 0 L BIPA CS2 R 0 L	0–255 (Row 0)
0	1	BIPA CS1 R 1 L BIPA CS2 R 1 L	256–511 (Row 1)
1	0	BIPA CS1 R 2 L BIPA CS2 R 2 L	512–767 (Row 2)
1	1	BIPA CS1 R 3 L BIPA CS2 R 3 L	768–1023 (Row 3)

If the current memory access operation is a DATI, the action of addressing a given location enables the memory circuits comprising that location and places the data stored in the addressed location on lines MEM SA ⟨17:00⟩ to the M8110 control.

3.4 M8110 SEMICONDUCTOR MEMORY CONTROL MODULE

Figure 3-3 is detailed block diagram of the M8110 control. Note that transfer of data through the M8110 to and from the Unibus or Fastbus and the associated memory matrix moudule is directed by the timing and control logic shown on drawing SMCA. This logic within the M8110 interprets control signals from the Fastbus or Unibus, controls communication with these buses, and implements DATO and DATI cycles when requested. The MOS memory refresh logic on the M8110 control is enabled through a jumper connection so that this logic is operational only when MOS memory matrix modules are controlled by the M8110 control.

Detailed descriptions of M8110 logic operation are divided into the following sections:

a. The selection, interface, bus, and diagnostic subfunctions, manipulated by the M8110 control logic to perform memory access cycles and system maintenance

b. The M8110 control logic

c. The M8110 refresh logic which applies only to MOS memory systems

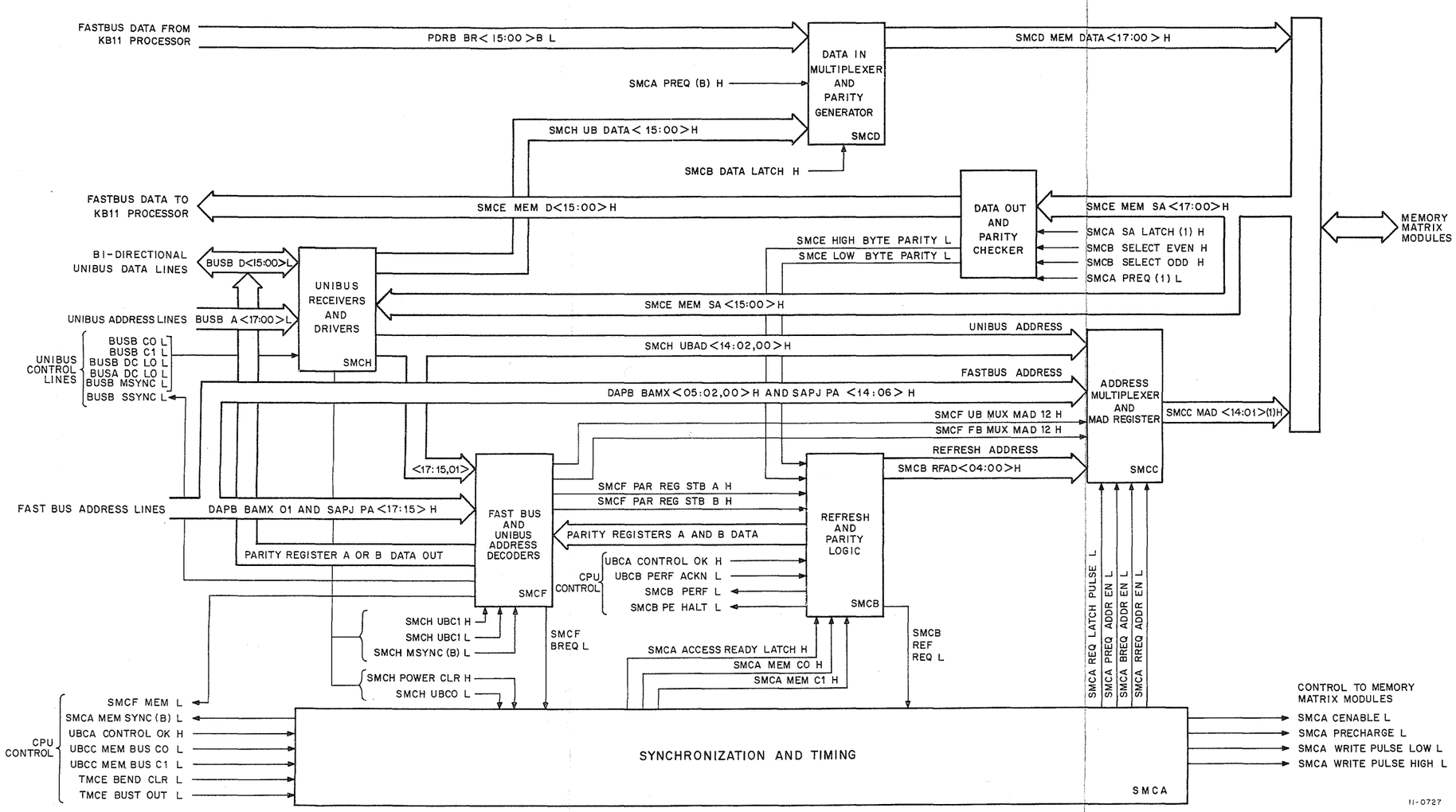


Figure 3-3 M8110 Semiconductor Memory Control Module, Block Diagram

3.4.1 Memory Selection Logic

Memory addresses from the Fastbus or Unibus are received in the M8110 control address selection logic (drawing SMCF) where they are decoded at a jumper-wired decoding matrix. Decoding of the states of address bits 11 through 17 determines if an address is within the previously extablished address range, i.e., the address is valid at this controller and memory will be accessed. In a PDP-11/45 System, address bits 17 and 16 address one of four 32K-word sections of memory. Because bit 15 addresses one of two 16K-word groups within a 32K-word section, the state of this bit designates the specific control being addressed. Address bits 14 and 13 specify, for a control with 16K words of MOS memory, that the location being addressed is within one of the four G401 MOS matrix modules. For a control with 4K of bipolar memory, the jumpered states of address bits 13 and 14 allow placement of a 4K-word set of contiguous addresses within a total set of 32K-word addresses. Jumper connection of bits 11 and 12 allow selection of 1K out of 4K decoded for one of four bipolar matrix modules.

Table 3-7 correlates the states of address bits 13 through 17 to the associated memory areas. The required jumper configurations are also shown.

A valid or acceptable memory address from the Fastbus is indicated by SMCF MEM L being returned to the processor via the Fastbus. This signal is the output of a wired AND configuration whose inputs are five exclusive-NOR gates, E89, and four NAND gates, E77. The address configuration and the absence or presence of jumpers C, D, E, F, H, J, K, L, and M determines SMCF MEM L generation. The jumpers are located at the input to the NOR gates and the output of the NAND gates.

As indicated in Table 3-7, retaining or removing the jumpers establishes the memory range controlled by address bits 13 through 17. Removal of a jumper (C, D, E, F, or H) will cause the associated address bit, when equal to a 1 (high), to disable the NOR gate and provide one of the required (high) "AND" inputs for SMCF MEM L. Likewise, retaining a jumper results in a 0 address bit disabling the particular NOR gate to provide another high input to the wired AND. A simplified version of the address decoder is depicted in Figure 3-4. The assertion of SMCF MEM H results from all high inputs to the wired AND. Highs from the exclusive-NOR gates result when both inputs are low or both inputs are high, thereby disabling the gates. It can be concluded from this that jumper presence (a low) allows a 0 bit (a low) to disable the gate; the gate is wired to accept a 0 address bit. Likewise, jumper absence allows 1 bits to be accepted. Highs from the NAND gates result when the jumper is cut (an address within the acceptable range, enabling the gate, is prevented from inhibiting SMCF MEM H) or, if the jumper is in place, not to have an address configuration (and address outside the acceptable range) that enables the gate.

NOTE

Jumpers F and H are applicable to bipolar memory only; they are left intact for MOS memory addressing.

Table 3-8 lists those address bits (11 and 12 for bipolar, 13 and 14 for MOS) and jumpers that pertain to the memory address range assignment of individual G401 MOS and M8111 bipolar matrix modules. The removal of any one jumper assigns the corresponding address range to a MOS or bipolar module. However, most memory configurations consist of more than one memory module. Table 3-9 lists those jumpers that must be removed to assign memory addresses to the given capacity memory. It is assumed that the user does not wish to omit assignment of any low-order addresses. For example, an 8K MOS memory of two modules would be assigned addresses 0–8191 by removing jumpers J and K. (Removing jumpers L and M would assign addresses 8192–16383 to the same module). It should be noted that these jumpers (J, K, L, and M) are used to assign addresses to individual matrix modules under the direction of a particular M8110 control, whereas jumpers C, D, E, F, and H are used to assign a 16K (for MOS) or a 4K (for bipolar) memory block to a M8110 control from the total (128K) address area.

Table 3-7

Fastbus/Unibus Memory Address (Assign and Decode)

Fastbus/Unibus Address Decoder Bits					Memory Address Assignment		M8110 Jumpers (E87) (NOTE 1, NOTE 2)				
17	16	15	14	13	Bipolar	MOS	C	D	E	F	H
0	0	0	0	0	0–4K	0–16K					
0	0	0	0	1	4–8K						X
0	0	0	1	0	8–12K					X	
0	0	0	1	1	12–16K					X	X
0	0	1	0	0	16–20K	16–32K			X		
0	0	1	0	1	20–24K				X		X
0	0	1	1	0	24–28K				X	X	
0	0	1	1	1	28–32K				X	X	X
0	1	0	0	0	32–36K	32–48K		X			
0	1	0	0	1	36–40K			X			X
0	1	0	1	0	40–44K			X		X	
0	1	0	1	1	44–48K			X		X	X
0	1	1	0	0	48–52K	48–64K		X	X		
0	1	1	0	1	52–56K			X	X		X
0	1	1	1	0	56–60K			X	X	X	
0	1	1	1	1	60–64K			X	X	X	X
1	0	0	0	0	64–68K	64–80K	X				
1	0	0	0	1	68–72K		X				X
1	0	0	1	0	72–76K		X			X	
1	0	0	1	1	76–80K		X			X	X
1	0	1	0	0	80–84K	80–96K	X		X		
1	0	1	0	1	84–88K		X		X		X
1	0	1	1	0	88–92K		X		X	X	
1	0	1	1	1	92–96K		X		X	X	X
1	1	0	0	0	96–100K	96–112K	X	X			
1	1	0	0	1	100–104K		X	X			X
1	1	0	1	0	104–108K		X	X		X	
1	1	0	1	1	108–112K		X	X		X	X
1	1	1	0	0	112–116K	112–128K	X	X	X		
1	1	1	0	1	116–120K		X	X	X		X
1	1	1	1	0	120–124K		X	X	X	X	
1	1	1	1	1	124–128K		X	X	X	X	X

NOTES: 1. "X" denotes jumper to be cut.

2. Jumpers F and H are left intact for all MOS memory assignments.

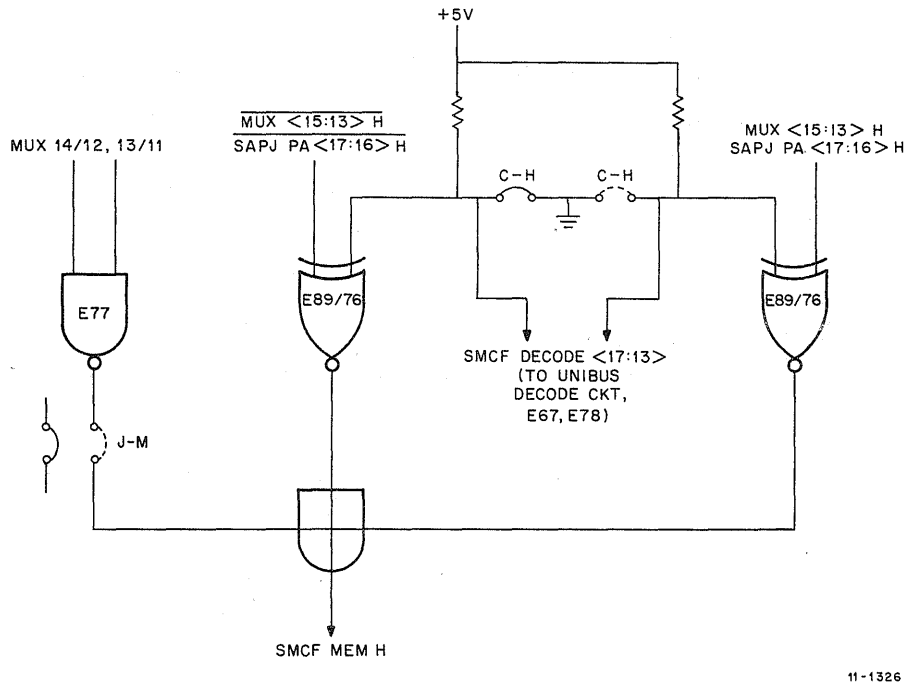


Figure 3-4 Simplified Memory Address Decode (SMCF)

Table 3-8
MOS/Bipolar Module Addressing

Fastbus/Unibus Memory Address Bits		Memory Address Assignment		Remove Jumpers	
FB MUX 14/12	FB MUX 13/11	MOS	Bipolar	Fastbus Address Select	Unibus Address Select
0	0	0–4095	0–1023	J	N
0	1	4096–8191	1024–2047	K	P
1	0	8192–12287	2048–3071	L	R
1	1	12288–16383	3072–4095	M	S

Table 3-9
MOS/Bipolar Memory Addressing

No. of Memory Modules in Memory*	Memory Capacity		Remove Jumpers	
	MOS	Bipolar	Fastbus Address Select	Unibus Address Select
1	4K	1K	J	N
2	8K	2K	JK	NP
3	12K	3K	JKL	NPR
4	16K	4K	JKLM	NPRS

*Connected to one M8110 Control.

starting at 16K boundary

Cut B, C on MOS board

The aforementioned jumpers are physically located on the M8110 module at locations E87 and E75. For example, as indicated on drawing SMCF, jumper J can be found at E75, terminal 01.

The inputs to the four NAND gates, E77, in the Fastbus address decoding circuit are SMCF FB MUX 14/12 H and SMCF FB 13/11 H. They are derived from a jumper-wired multiplexer, E67, located on the M8110 module. Whether address bits 11 and 12 or 13 and 14 are used is determined by the memory type; bits 11 and 12 select a 1K section out of a 4K memory area for bipolar, while bits 13 and 14 select a 4K section out of a 16K area for MOS (Table 3-8). Figure 3-5 illustrates the required jumper connections for both memory types. Memory address bits 13 and 14 (SMCF FB MUX DEC 13, 14 H) are also input to decoder NOR gates E76 and E89 from this same multiplexer, E67. Again, the memory type determines the address bit origin. Note that in the MOS configuration, with jumpers F and H retained, the jumper inputs to NOR gates E76 and E89 (bits 13 and 14) are always at ground. The address bit inputs to these same gates are jumpered, at E67, to the F and H jumper inputs (SMCF DECODE 13, 14 H), thereby disabling the gates (all inputs are at ground). Since the output from these two NOR gates is always high, effectively removing them from the decoder, the influence of bits 13 and 14 in MOS memory addressing depends on the absence or presence of jumpers J, K, L, and M.

The SMCF FB MUX MAD 15 H input to NOR gate E89 of the Fastbus address decoder is from another jumper-wired multiplexer, E86, on the M8110 module. Figure 3-6 shows the jumper configuration required to route Fastbus/Unibus address bit 15 to the address decoder.

An effective Unibus memory address, together with SMCH MSYNC (B) L, generates the SMCF BREQ L signal that initiates a Unibus DATO or DATI operation. The Unibus address decoder (SMCF) is a wired-AND circuit, similar to the Fastbus address decoder described above, that consists of five NAND gates, E74 and E85, and five exclusive-NOR gates, E76 and E88. Inputs to the NOR gates are SMCF MUX MAD 15 from E86 (Figure 3-6), Unibus address bits 16 and 17, and SMCF UB MUX DEC 13, 14 H from E78, a jumper-wired multiplexer on the M8110 module. E78 is wired (Figure 3-7) according to the memory type installed; it performs the same function for Unibus addressing as E67 does for Fastbus addressing. Inputs to the four NAND gates, E74 (SMCF UB MUX 13/11, 14/12 H), are also from E78. Unibus decoder bits 13 through 17 (NOR gates E76 and E88) use the same jumper (C, D, E, F, and H) configuration established for Fastbus addressing. In addition, jumpers N, P, R, and S on the output of NAND gates E74 must be selectively removed (Tables 3-8 and 3-9) to establish the desired memory addresses for the matrix modules. Jumpers N, P, R, and S are located at the same physical location, E75, as jumpers J, K, L, and M of the Fastbus address decoder.

3.4.2 Unibus Interface (SMCH)

Figure 3-3 shows the Unibus data and address paths. In contrast to the Fastbus which, along with a semiconductor memory, is a physical component of the PDP-11/45 processor, the Unibus can be located remotely. As a consequence, the M8110 can connect to the full-duplexed Unibus through long lines which must be driven and received. The Unibus receiver and driver logic (shown on drawing SMCH) includes: the address receiving logic involved in both DATO and DATI cycles, the data receiving logic which operates only on a DATO, the data driving logic which responds to a DATI operation, and specific logic signals controlling Unibus DATO and DATI operations.

The 18-bit Unibus address received at SMCH on the lines BUSB A ⟨17:00⟩ L is input to an 18-stage buffer formed by type 380 line receivers, AND gates E48, E66, E96, E110, and E121. The second input to each receiver is conditioned by a common line to ground. Therefore, each Unibus address received is terminated at the characteristic line impedance and inverted to assert SMCH UBAD ⟨17:00⟩ H. These outputs are applied to the MAD register shown on SMCC.

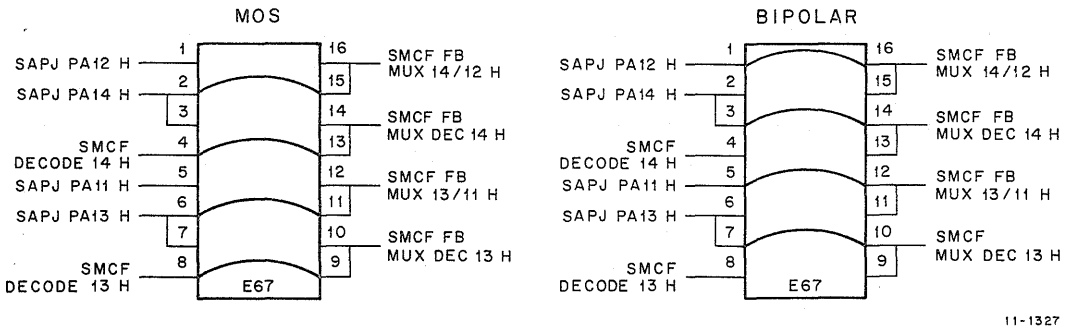


Figure 3-5 Fastbus Address Multiplexing ⟨14:11⟩
Required E67 Jumpers

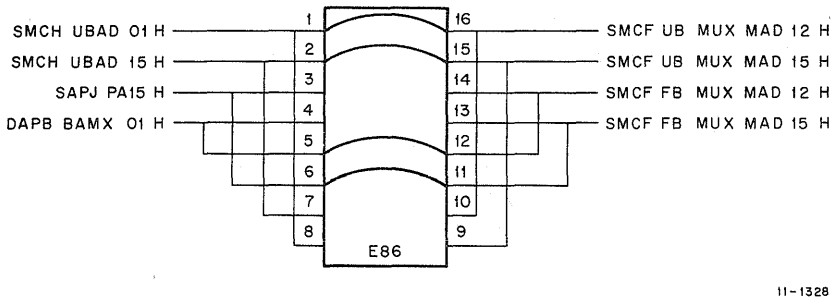


Figure 3-6 MAD Multiplexing, Required E86 Jumpers

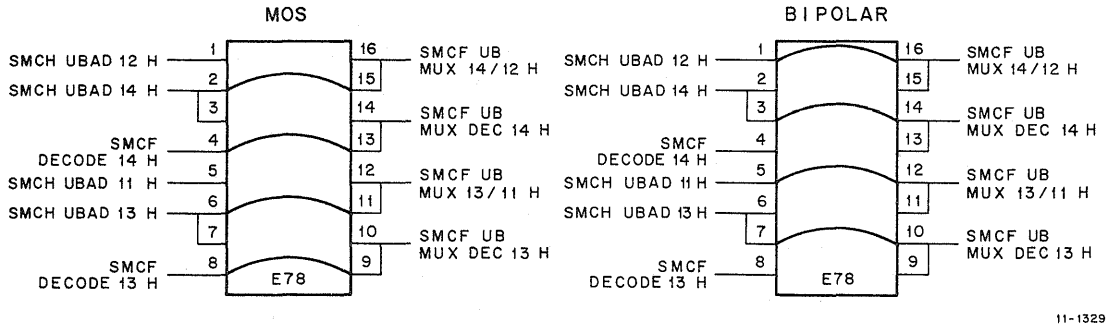


Figure 3-7 Unibus Address Multiplexing ⟨14:11⟩
Required E78 Jumpers

The 16-bit Unibus data input is received at SMCH on the lines BUSB D ⟨15:00⟩ L as input to a 16-stage buffer formed by type 380 line receivers, AND gates E32, E33, E34, and E35. The second input to each receiver is conditioned by a common line to ground. As a result, each data word received from the Unibus is terminated at the characteristic line impedance and inverted to assert SMCH UB DATA ⟨15:00⟩ H. These outputs are applied to data in the multiplexer as shown on SMCD.

The data word read during a given DATI cycle is asserted at the Unibus interface as SMCE MEM SA ⟨15:00⟩ H. This data is input to a 16-stage drive network formed by type 8881 open collector NAND gates, AND gates E44, E45, E46, and E47. This gating network is enabled by the ANDing of SMCB MEM SSYNC L and SMCH UBC1 H. SMCH UBC1 H is low during DATI operations and SMCB MEM SSYNC L is asserted during each DATI cycle at the point where the data word addressed during that cycle is stable. The output of this gating network, when enabled, asserts the line BUSB D ⟨15:00⟩ L on the Unibus.

All Unibus control signals to the M8110 are received and buffered at SMCH. BUSB MSYNC L is received at the Unibus interface and inverted to assert SMCH MSYN (B) H (E96). This level is, in turn, inverted to assert the complementary signal SMCH MSYN (B) L at E100.

BUSB C0 L and C1 L define the nature of each Unibus access cycle. They are received and inverted to generate SMCH UBC0 H, L at E36 and E38 and SMCH UBC1 H, L at E48 and E38. The latter signal is inhibited until SMCH MSYNC (B) L (E100) is received 150 ns after the processor raises BUS BUSY. The states of SMCH UBC0 and SMCH UBC1, along with the memory operation initiated by each state, are listed in Table 2-2. Note that the levels of UBC0 L and UBC1 L correspond directly with the C0L and C1L levels from the Unibus, while the UBC0 H and UBC1 H levels are complementary to the Unibus inputs.

PWRS MEM DC LO L is received at the interface and inverted to assert one of the OR conditions for SMCH POWER CLR L. BUSB INIT L is received at the Unibus and gated with the AND of SMCB REF REQ L and SMCA RREQ (B) L. The result, when true, is the other OR condition that asserts SMCH POWER CLR L. The purpose of this level is to clear all condition-sensitive logic following a power-up cycle and to initialize this logic at start-up time. Note that if a refresh cycle is in process, SMCH POWER CLR L is inhibited, except when a power failure causes PWRS MEM DC LO L to be asserted.

NOTE

Fastbus address and data interfacing are shown, respectively, on drawings SMCC and SMCD. These drawings are described in Paragraphs 3.4.3 and 3.4.4.

3.4.3 Address Multiplexing (SMCC)

The semiconductor memory bus is part of the M8110 control and includes the multiplexing of memory address and data from the Fastbus and Unibus to the memory matrix modules. Data addressed on a DATI cycle is bussed directly from the matrix modules to both the Fastbus and Unibus interfaces to be received by the requesting bus (Fastbus or Unibus). Refer to the data and address path block diagram shown in Figure 3-3. The M8110 address multiplexing logic, shown on drawing SMCC, is shared by three classes of addresses: the Unibus address, the Fastbus address, and the refresh address.

NOTE

Refresh addresses are generated only when an M8110 is controlling G401 MOS Memory Matrix modules. When an M8110 is controlling M8111 Bipolar Memory Matrix modules, the logic that generates refresh addresses is disabled.

Out of each 18 address bits received at the control from either the Unibus or Fastbus, 15 bits are multiplexed and mapped as shown in Figure 2-7 and Table 3-10. The refresh address SMCB RFAD ⟨04:00⟩ H is a row address only and is internally generated (Paragraph 3.4.8).

Address multiplexing occurs asynchronously, based either on demand, as with isolated access requests, or on priority arbitration, as in the case of several simultaneous access requests. However, when the multiplexing strobe levels are asserted at the address multiplexing logic, all priority claims have been arbitrated; subsequent requests are locked out. The previous address is output until the leading edge of SMCA REQ LATCH PULSE L, when it is unlatched from the buffer.

Table 3-10
Multiplexed Address Inputs to MAD (SMCC)

Unibus Address	Fastbus Address		Refresh Address		Memory Address
SMCH UBAD XX H	SAPJ PA XX H	DAPB BAMX XX H	SMCB MAD XX (1) H, L		SMCC MAD XX (1) H, L
00		00		→	00
02		02		→	01
03		03		→	02
04		04	00	→	03
05		05	01	→	04
06	06		02	→	05
07	07		03	→	06
08	08		04	→	07
09	09			→	08
10	10			→	09
11	11			→	10
12	12			→	11
01 (NOTE 1)		01 (NOTE 2)		→	12
13	13			→	13
14	14			→	14
15 (NOTE 3)	15 (NOTE 4)				
16	16				
17	17				

NOTES:
1. Asserts SMCF UB MUX MAD 12 H
2. Asserts SMCF FB MUX MAD 12 H
} → MAD 12
3. Asserts SMCF UB MUX MAD 15 H
4. Asserts SMCF FB MUX MAD 15 H

3.4.3.1 **Unibus Address Multiplexing** – SMCA BREQ (B) H and SMCA REQ LATCH PULSE H (drawings SMCA and SMCC) assert SMCA BREQ ADDR EN L to gate SMCH UBAD ⟨14:00⟩ H and SMCF UB MUX MAD 12 into the latching buffer. This address from the Unibus is latched into the buffer on the trailing edge of SMCA REQ LATCH PULSE L. This serves to map the address so the SMCH UBAD ⟨12:02⟩ correspond to MAD ⟨11:01⟩ (1) H, SMCF UB MUX MAD 12 H corresponds to SMCC MAD 12 (1) H, SMCH UBAD ⟨14:13⟩ H correspond to SMCC MAD ⟨14:13⟩ (1) H, and SMCH UBAD 00 H corresponds to SMCC MAD 00 (1) H.

3.4.3.2 **Fastbus Address Multiplexing** – Fastbus addresses are multiplexed onto the address latching bus by SMCA PREQ ADDR EN L, which is asserted by SMCA PREQ (B) H and SMCA REQ LATCH PULSE H. This action gates the Fastbus address inputs onto the address latching bus. This address data is latched into the buffer on the trailing edge of REQ LATCH PULSE L. Fastbus addresses are mapped in the same manner as Unibus addresses.

3.4.3.3 **Refresh Address Multiplexing** – The 5-bit internally generated refresh address SMCB RFAD ⟨04:00⟩ H is multiplexed into the address latching buffer by the assertion of SMCA RREQ (B) L inverted, and latched on the trailing edge of SMCA REQ LATCH PULSE L. Each refresh address loaded into the buffer is mapped so that SMCB RFAD ⟨04:00⟩ H corresponds to MAD ⟨07:03⟩ (1) H.

3.4.4 Data Multiplexing (SMCD)

In executing a DATO operation from the Fastbus or Unibus, a data word or byte accompanies the memory address. Multiplexing of the data takes place in a 16-stage memory data buffer, with each stage driving the corresponding stage of a 16-stage latching data register. Logic is shown on drawing SMCD. Four 74S158 multiplexers (E10, E11, E20, and E23) comprise the data buffer; the latching data register is composed of three elements of a 3404 latch (E1, E3, and E12).

During a Fastbus DATO operation, data (PDRB BR ⟨15:00⟩ B L) is gated into the data buffer with SMCA PREQ (B) H. However, during a Unibus DATO, the absence of this signal ($\overline{\text{SMCA PREQ (B) H}}$) enables the data (SMCH UB DATA ⟨15:00⟩ H) entry. The output of each multiplexer stage is delivered to the data (D) input of the corresponding data latching register stage. SMCB DATA LATCH H is the common latching pulse to all the L inputs of this register for both Fastbus and Unibus write operations.

SMCD MEM DATA ⟨15:00⟩ H is output to memory for storage. The output of the data buffer, SMCD MBD ⟨15:00⟩, is also input to two parity generators, E2 and E4, whose outputs are the parity bits SMCD MEM DATA ⟨17:16⟩ H to memory. Odd or even parity generation is determined by the SMCB SELECT EVEN H and SMCB SELECT ODD H inputs to E2 and E4. The resultant output of E2 and E4 is latched into two latching register stages, E12, with SMCB DATA LATCH L. During DATO, both outputs of the parity generator are stored; bit 17 with the high-order byte and bit 16 with the low-order byte. Either of the two bits will be generated and stored when a DATOB is executed.

3.4.5 Data Output (SMCE)

Read data, destined for the Fastbus during DATI operation, is retained in the Data Out Register shown on drawing SMCE. This 18-stage logic circuit, composed of a latching register and an output buffer, functions as the interface when memory is read out to the Fastbus. Read data to the Unibus, bypassing this logic, is routed directly from memory to the Unibus drivers (drawing SMCH).

The 16 low-order stages of the Data Out Register are formed by three 3404 latch elements (E102, E111, and E122) and four 74S03 open-collector NAND gates (E101, E112, E113, and E123). Stages 16 and 17, which latch the lower and upper byte parity bits for input to the parity checking circuit (E103 and E124), are formed by two of the latches in E122.

The data (SMCE MEM SA ⟨17:00⟩ H) from the addressed memory location is inverted in the latching register and output to the parity checking logic as SMCE DATA OUT ⟨15:00⟩ L. Latching of the input data into the latching register occurs once during each DATI cycle when SMCA SA LATCH (1) H is raised. SMCE DATA OUT ⟨15:00⟩ L is, in turn, inverted in the output buffer and gated by SMCA PREQ (1) L onto the Fastbus as SMCA MEM D ⟨15:00⟩ H. The parity checker, E103 and E124, provides a parity check for each 8-bit byte. This circuit is conditioned by either SMCB SELECT EVEN H or SMCB SELECT ODD H, according to the selected parity mode. Output of the parity checker, SMCE LOW BYTE PARITY L and SMCE HIGH BYTE PARITY L, along with SMCE DATA OUT ⟨17:16⟩ L, is delivered to the parity compare logic (drawing SMCB) to determine whether a parity error exists.

3.4.6 M8110 Control Logic

The M8110 control logic (drawing SMCA) directs all aspects of a given memory access cycle, including priority arbitration, in response to a specific Fastbus or Unibus request. Description of SMCA control logic operation is based on the logic event sequence characteristic of DATO and DATI bus transactions. These event sequences apply to M8110 controls with either MOS or bipolar memory, with or without optional parity. In a system without byte parity, M8110 parity and diagnostic logic is ignored.

Because the semiconductor memory system can be accessed from either the Unibus or Fastbus, a DATO operation necessarily has two sources of data access initiation: one in response to Unibus DATO requests, and the other in response to Fastbus DATO requests. Both modes of DATO execution generally share a common control logic structure, with entrances to the logic being a function of the specific request. This same structure also serves to implement the intermally initiated refresh cycle, which is applicable only to a MOS memory system.

In a DATI cycle, the location is addressed and the data in that location is read and transferred to the Unibus or Fastbus. However, a DATIP implements a pause after the data is read and transferred, which locks out all other access cycle requests until the next access cycle is initiated. This next access cycle must be a DATO or DATOB. In all cases, the DATO following a DATIP will occur within one processor machine cycle. Like the DATO cycle, a DATI operation has two modes of initiation: one in response to a Unibus DATI request, and one in response to a Fastbus DATI request. Both modes of DATI execution generally share a common control logic structure with entrances to this logic being a function of the specific request.

Figures 3-8, 3-9, 3-10 and 3-11 are flow charts illustrating the sequential steps during DATO and DATI cycles from the Unibus and Fastbus to a MOS memory location. (Due to the similarity to MOS operation, bipolar flows are not shown. Differences can be seen where the signal BIPOLAR L is a factor.) The individual steps in the flow charts itemize events or conditions that are necessary for the completion of the entire DATO/DATI cycle. Required operations are shown by rectangular blocks, while necessary decisions are depicted by diamond-shaped blocks. A decision is resolved on the basis of the particular condition prevailing at the time the decision block is entered. AND and OR functions are shown, where necessary, to indicate the requisites for certain operations; off-page connectors provide intra-figure continuity. The remarks section contains comments relative to the particular step, signal requirements, and the logic drawing where the circuit can be found. Timing for the four types of cycles covered by the flow charts is shown in Figures 3-12, 3-13, 3-14 and 3-15. It is suggested that these timing diagrams be referenced while tracing through the flow charts.

3.4.7 Diagnostic Logic

The parity generation and checking feature of the MS11 Semiconductor Memory System is exercised by PDP-11/45 diagnostic programs that provide a principle technique of pinpointing memory malfunctions. The diagnostic logic consists of a parity register decoding structure (drawing SMCF), two identical diagnostic parity registers, and parity enabling logic (drawing SMCB). Figure 3-16 shows the relationship of these circuits to the read and write data routed through the Data Out and Data In Registers, respectively. The parity decoding logic for each control is hard-wired to decode only the addresses for the two diagnostic parity registers. As a result of decoding one of these addresses, the associated diagnostic parity register is enabled for either being read or written into. The access cycle which accomplishes this reading or writing is the same as any other Unibus access cycle except for the unique address.

The two 5-stage diagnostic parity registers have common input lines and separate output lines. By loading a register with a specific binary array, the diagnostic program can enable or disable parity error, specify odd or even parity for writing and/or reading in a given 4K of memory, enable or inhibit a halt on parity error, and enable or inhibit a time-out trap on parity error.

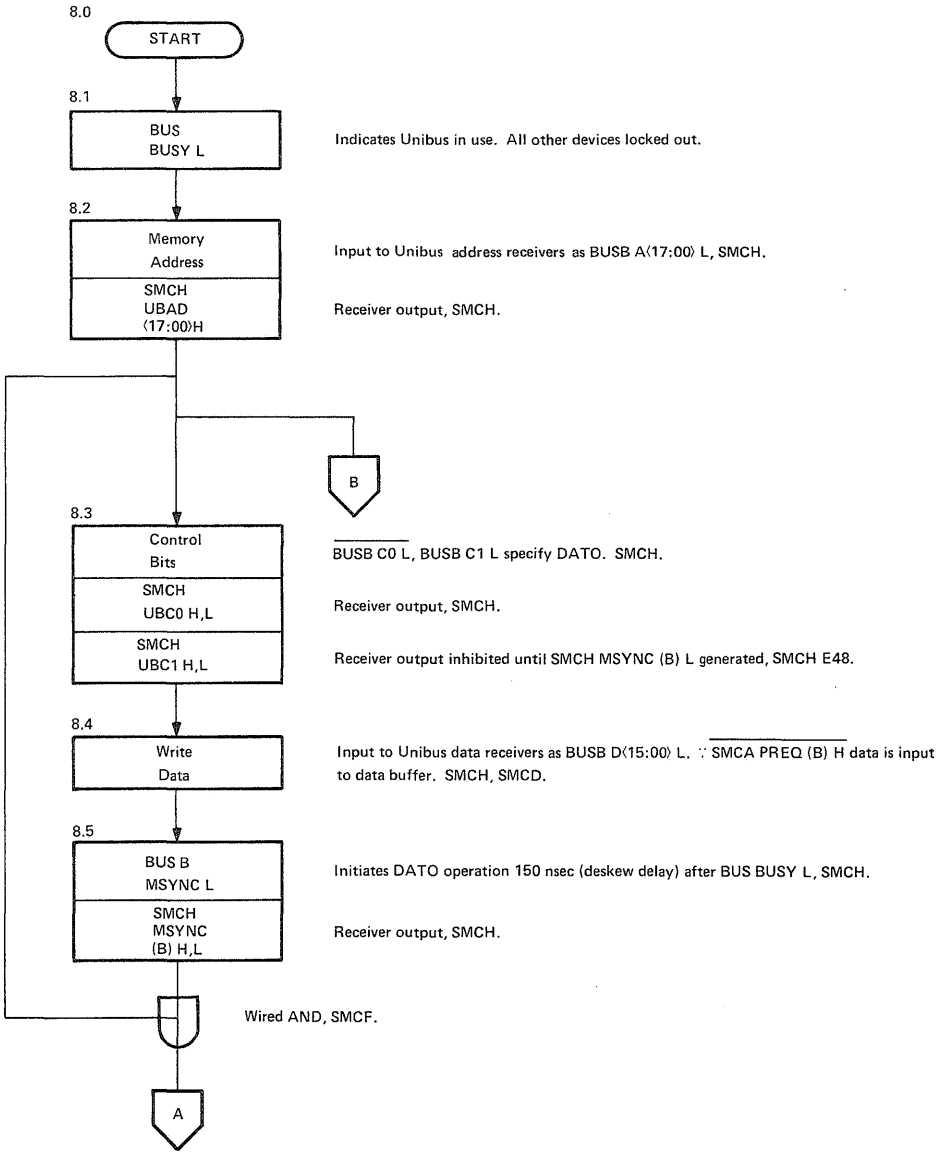


Figure 3-8 Unibus DATO Logic Flow (Sheet 1 of 7)

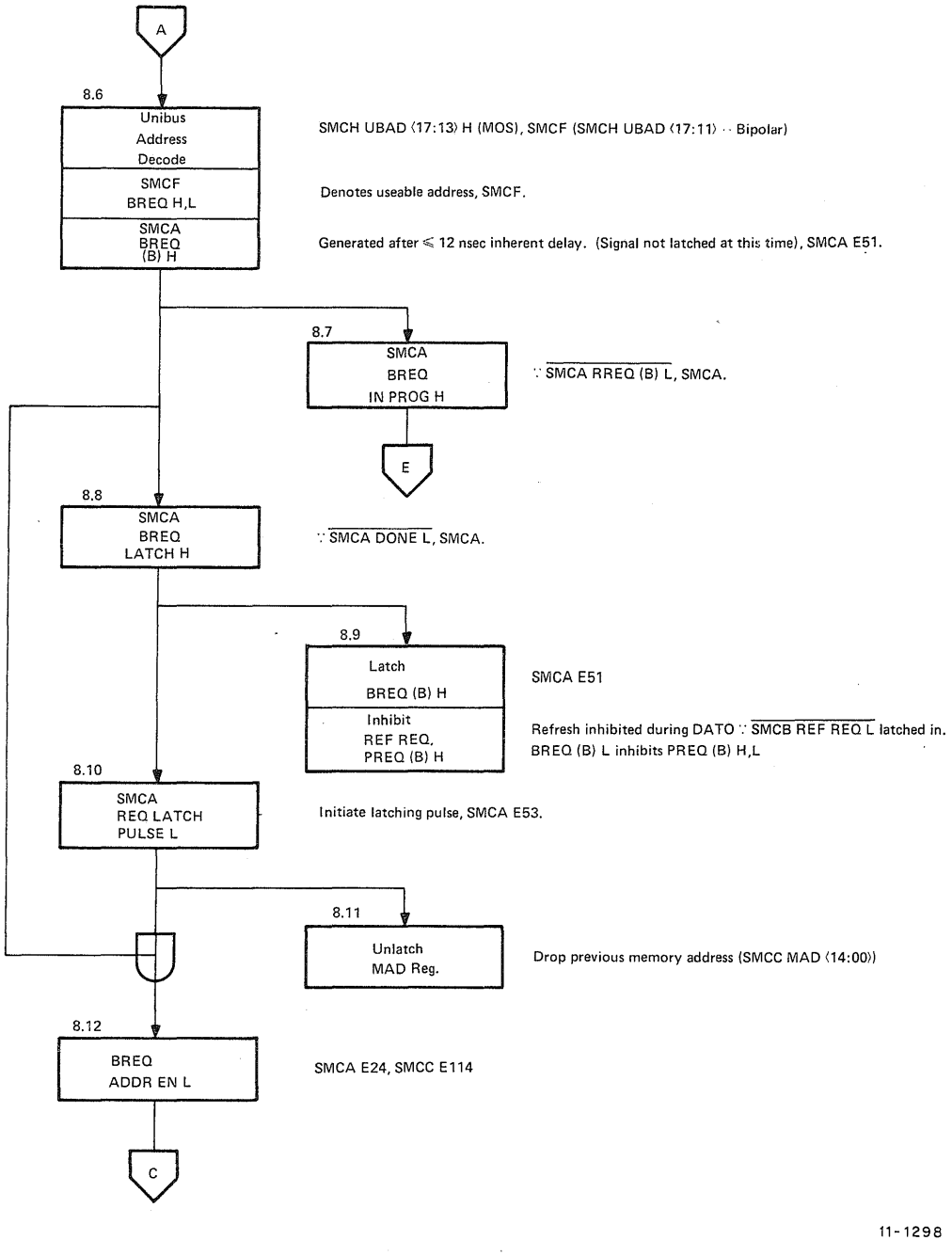


Figure 3-8 Unibus DATO Logic Flow (Sheet 2 of 7)

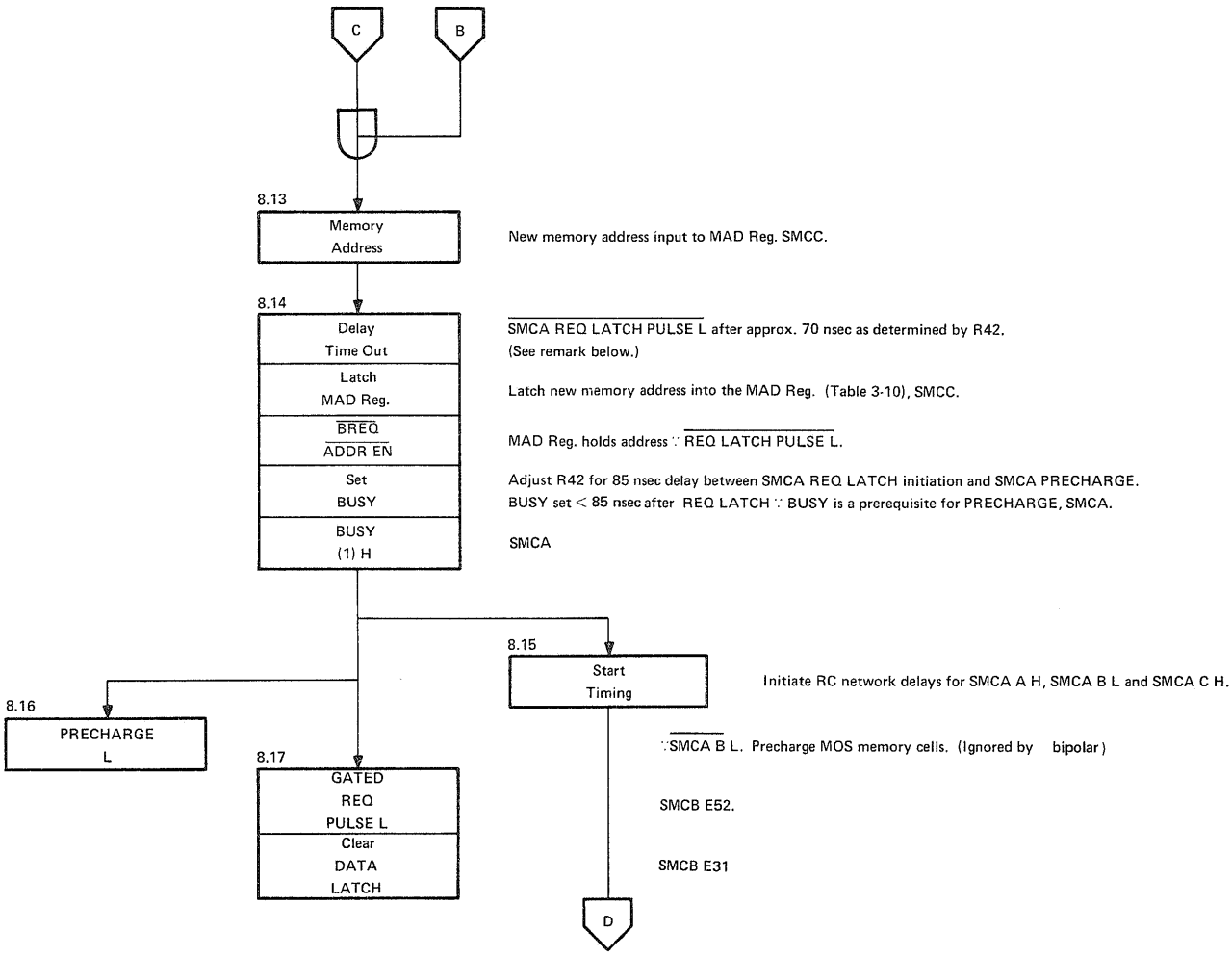


Figure 3-8 Unibus DATO Logic Flow (Sheet 3 of 7)

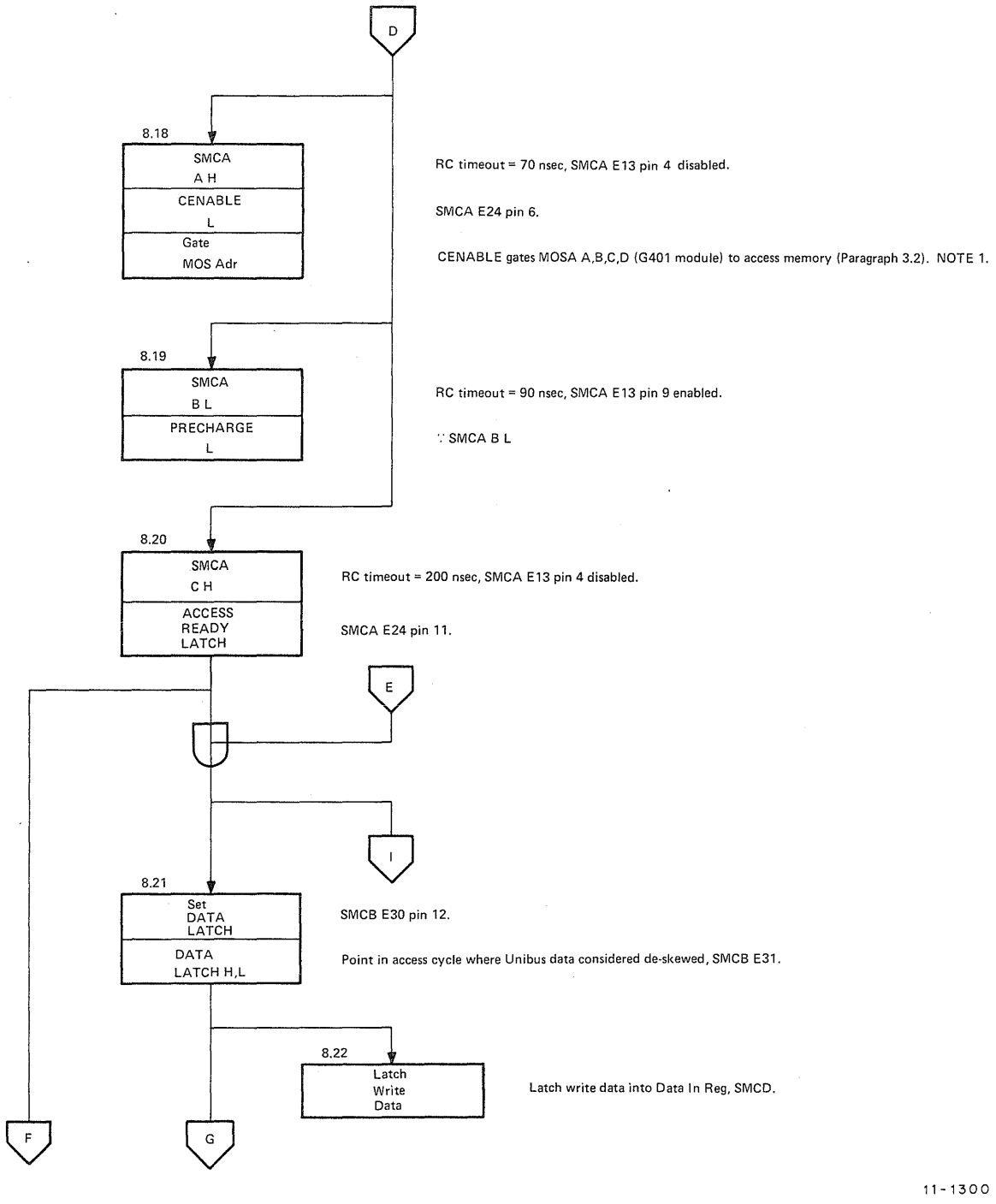


Figure 3-8 Unibus DATO Logic Flow (Sheet 4 of 7)

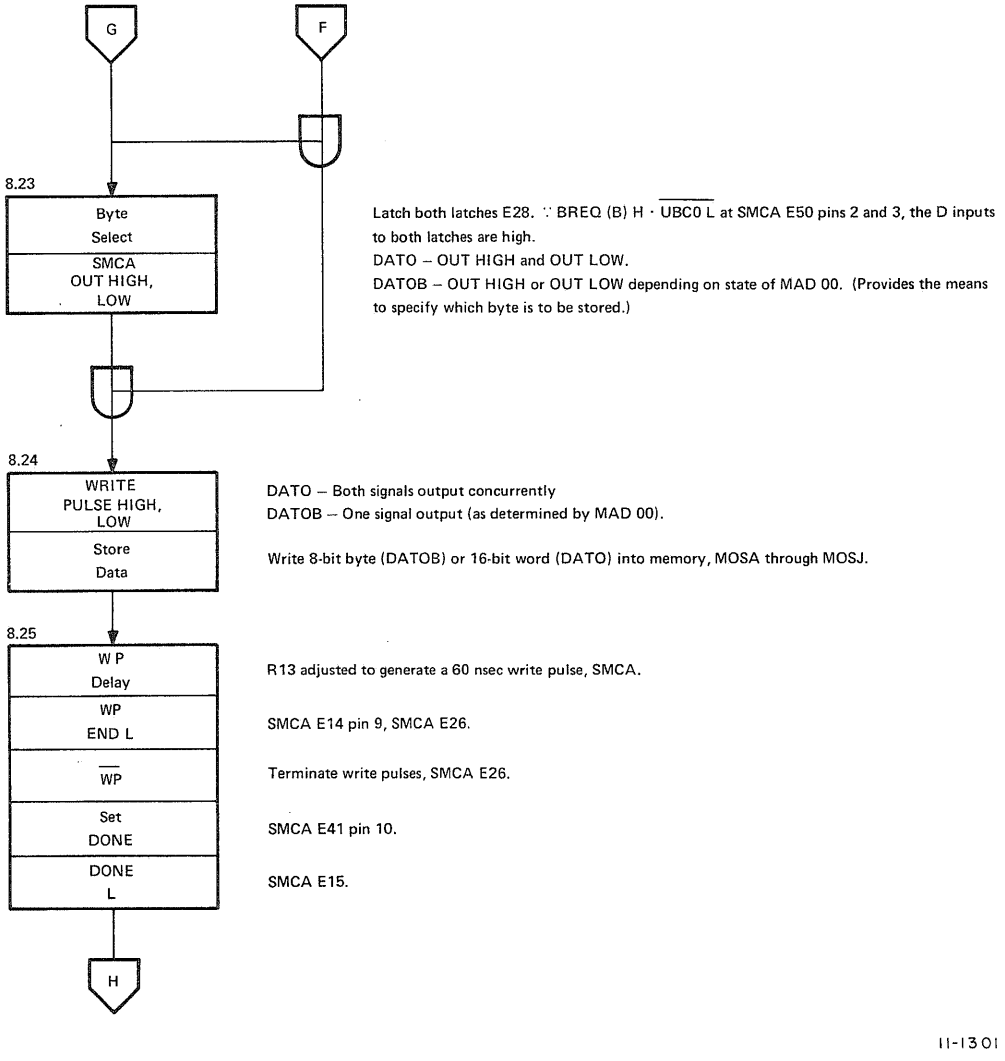


Figure 3-8 Unibus DATO Logic Flow (Sheet 5 of 7)

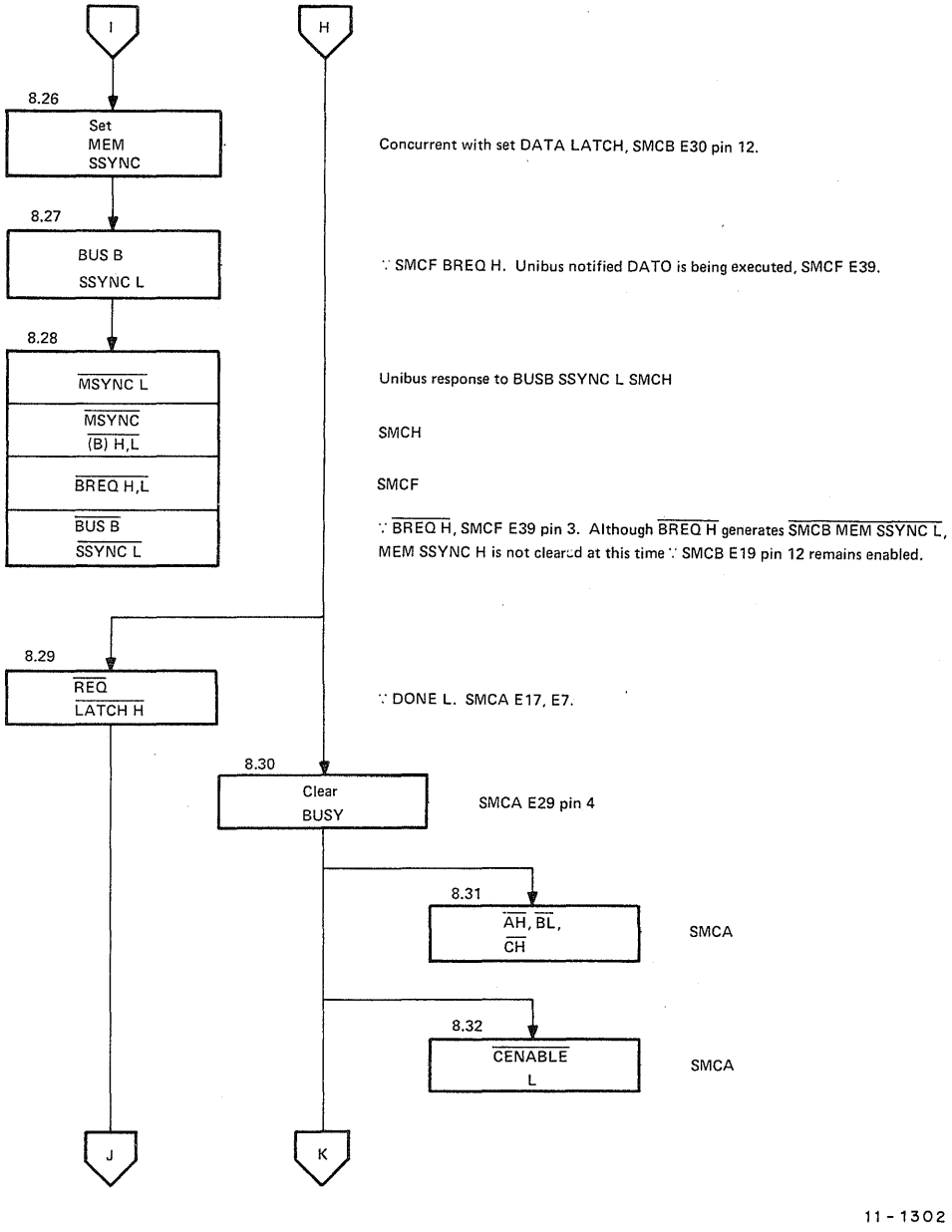
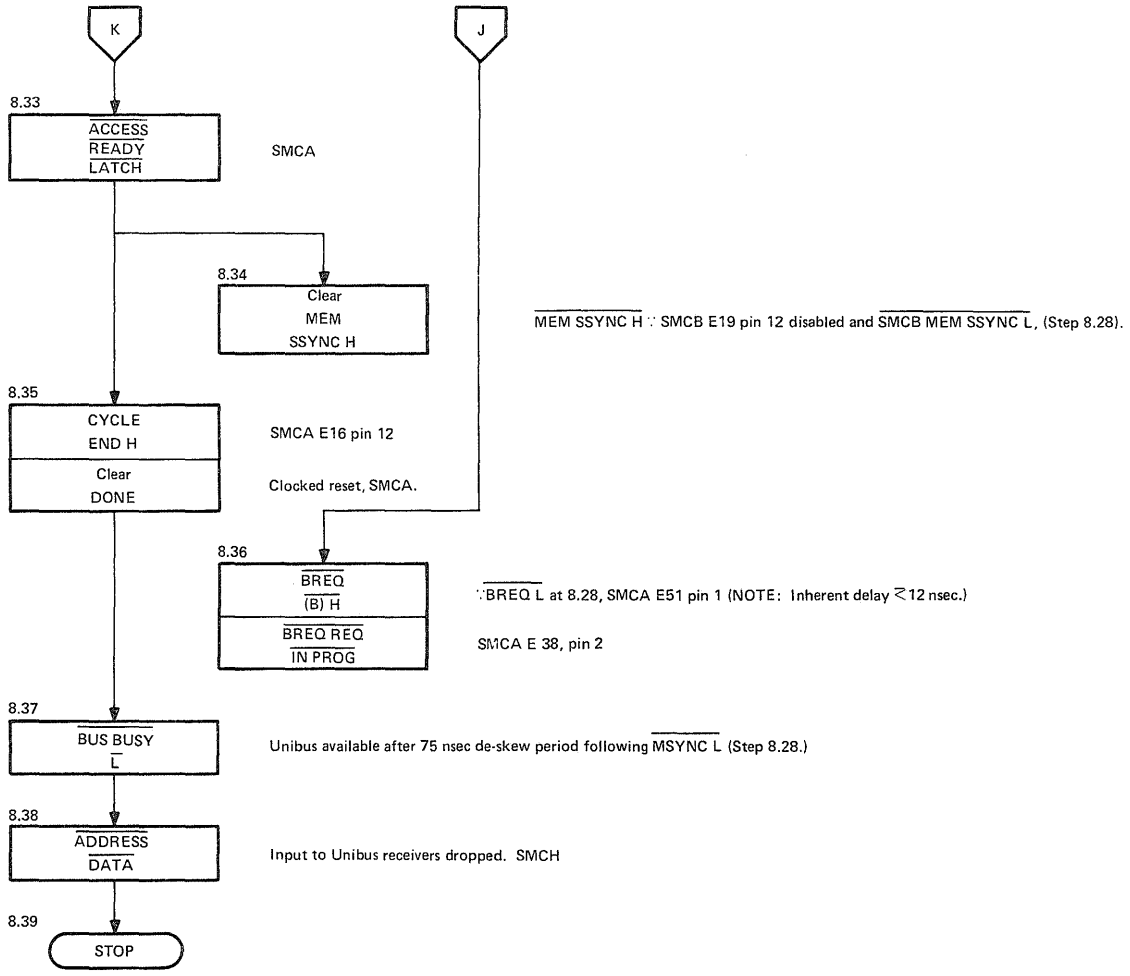


Figure 3-8 Unibus DATO Logic Flow (Sheet 6 of 7)



NOTE 1: If memory is bipolar , jumper A is not cut generating BIPOLAR L (SMCB). SMCA E13 pin 4 is never enabled. ∴ CENABLE L follows BUSY (1) H. CENABLE generates BIPB CS3 A, B, C, D on M8111 module (Paragraph 3.3.1.3).

11-1303

Figure 3-8 Unibus DATO Logic Flow (Sheet 7 of 7)

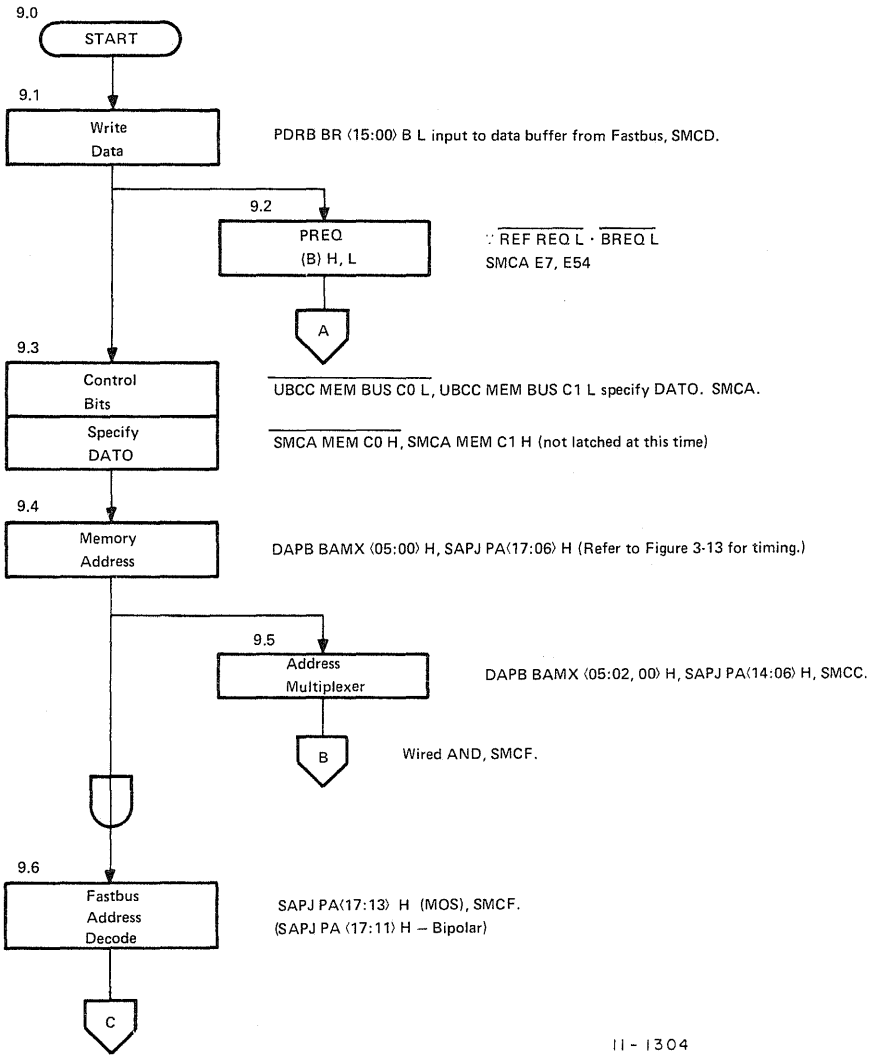


Figure 3-9 Fastbus DATO Logic Flow (Sheet 1 of 7)

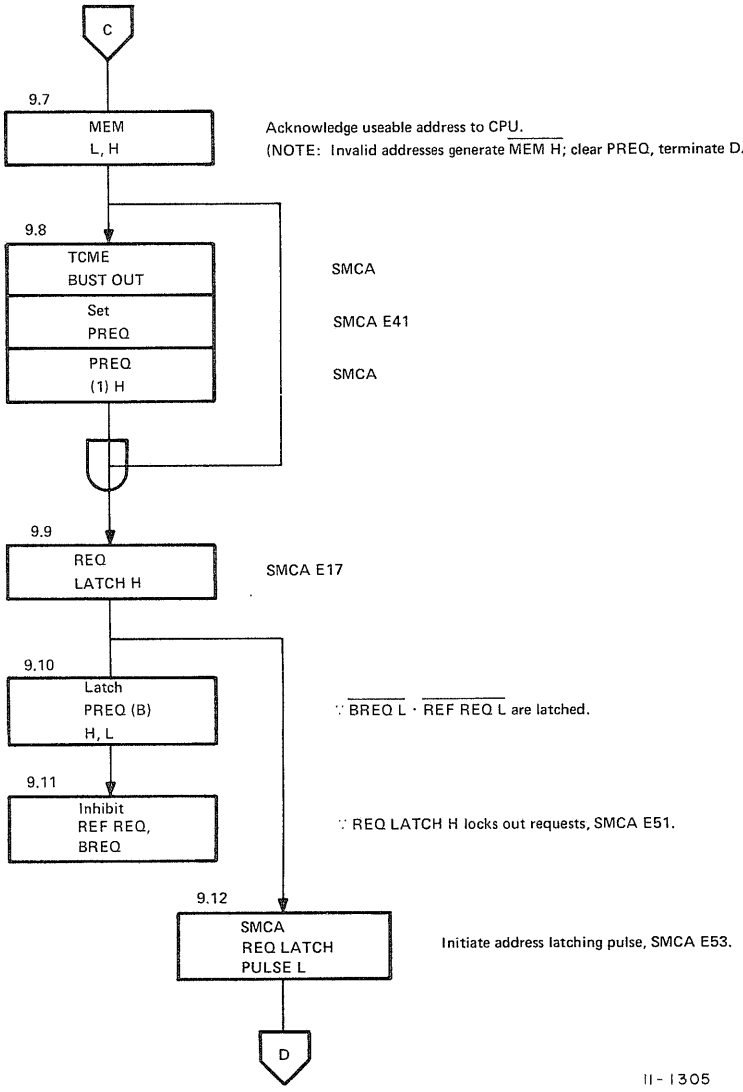


Figure 3-9 Fastbus DATO Logic Flow (Sheet 2 of 7)

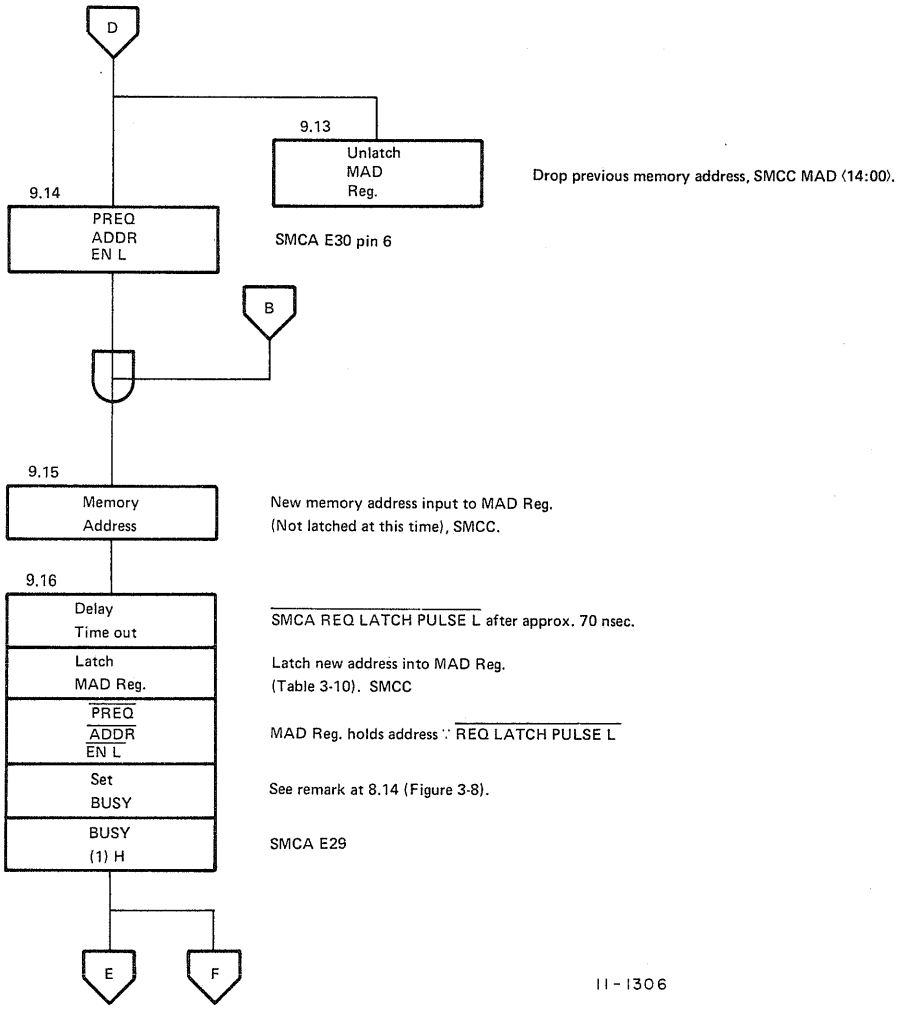


Figure 3-9 Fastbus DATO Logic Flow (Sheet 3 of 7)

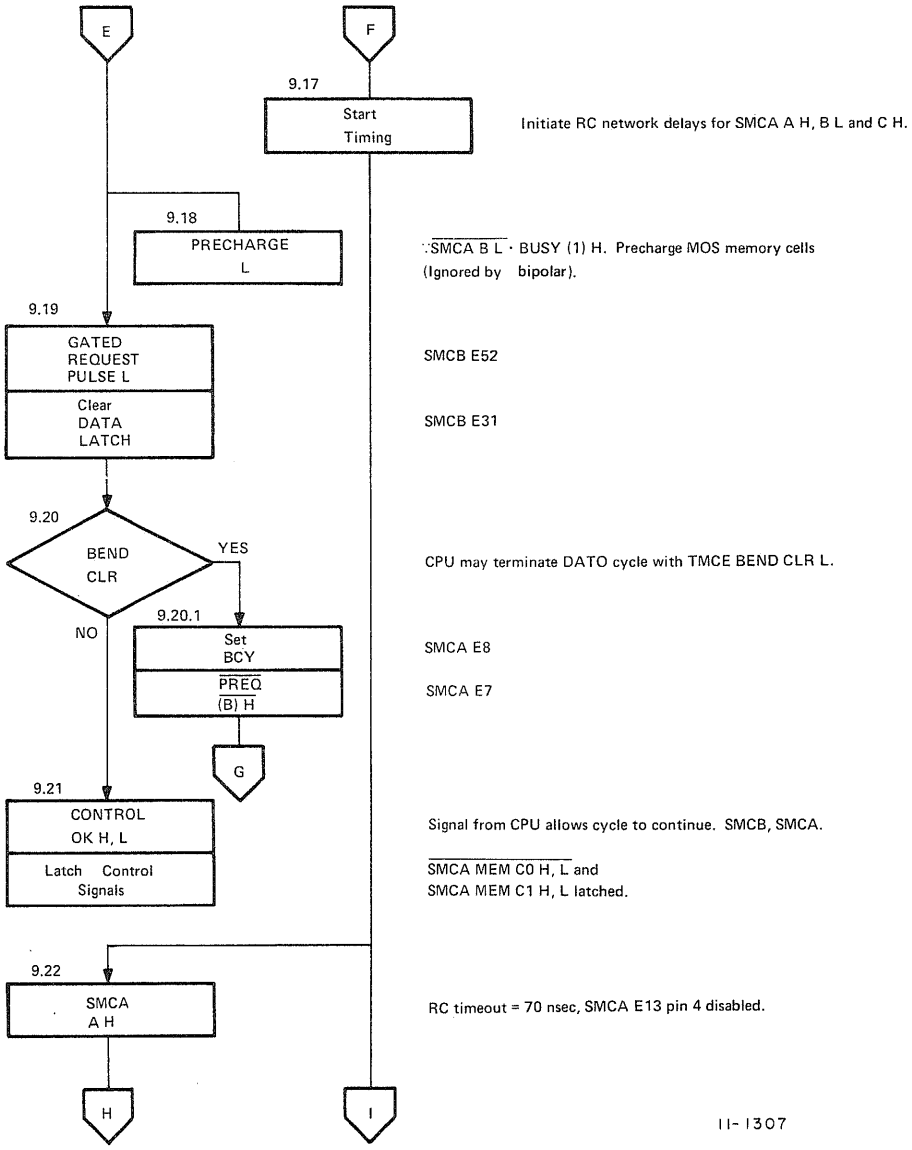


Figure 3-9 Fastbus DATO Logic Flow (Sheet 4 of 7)

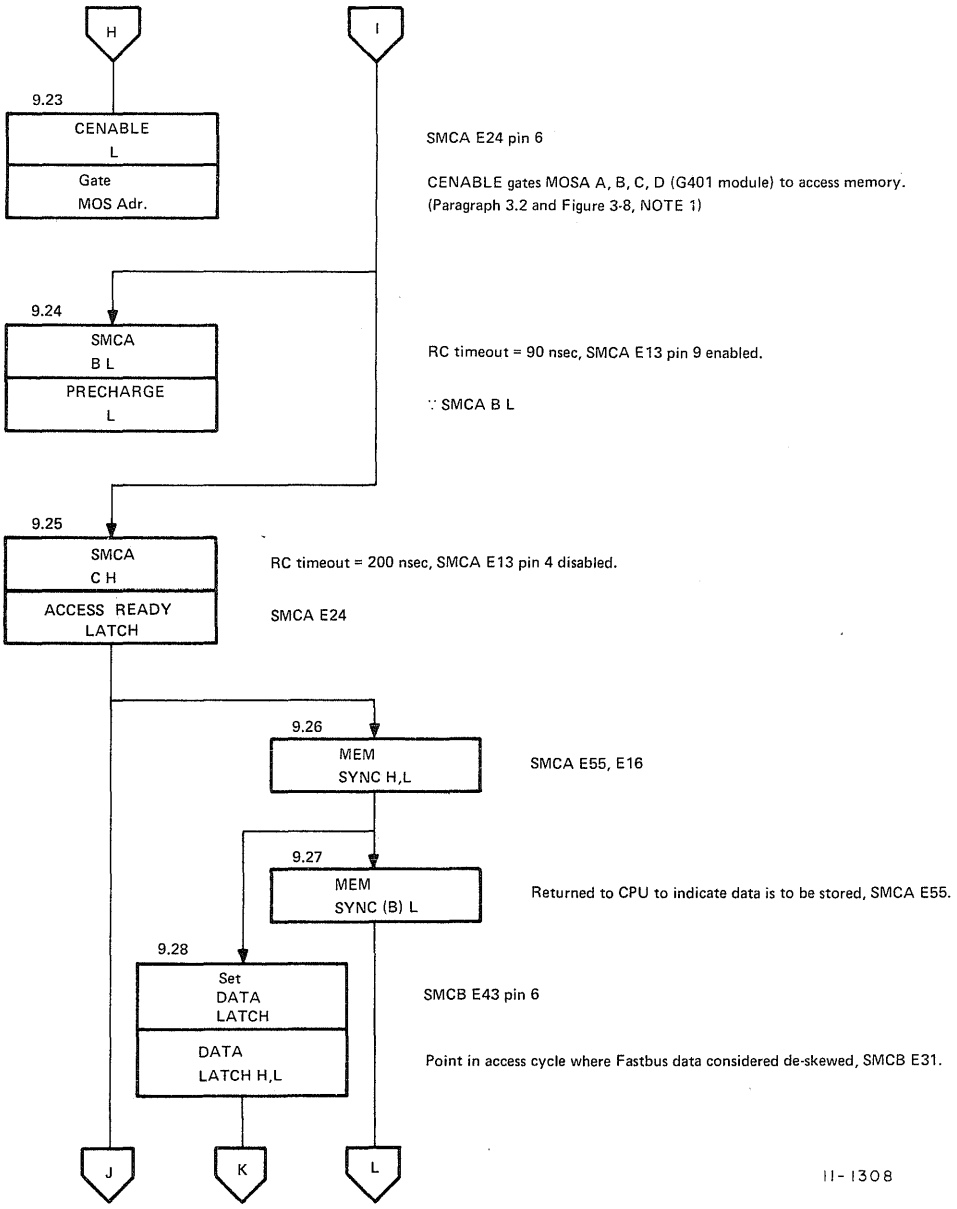


Figure 3-9 Fastbus DATO Logic Flow (Sheet 5 of 7)

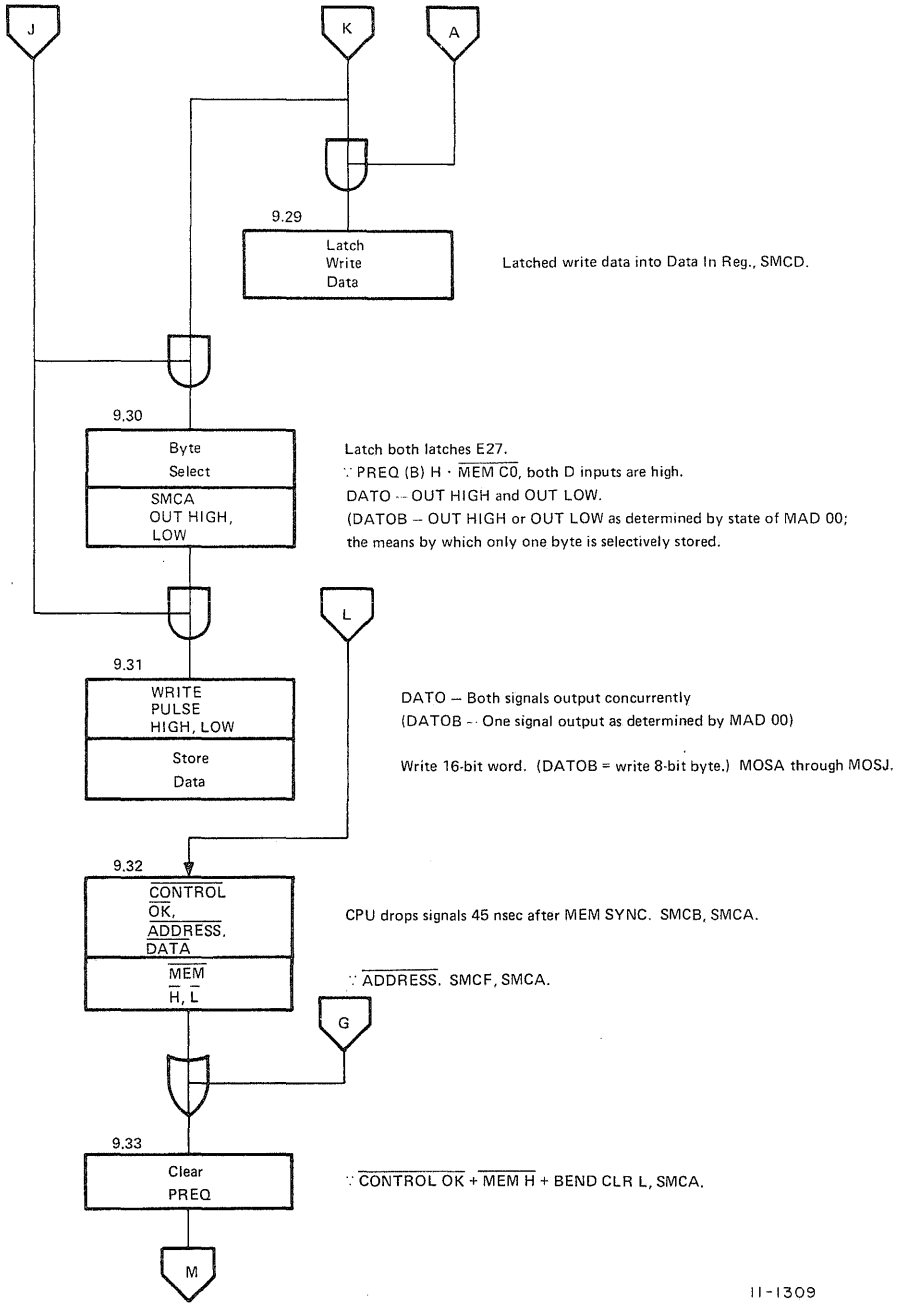


Figure 3-9 Fastbus DATO Logic Flow (Sheet 6 of 7)

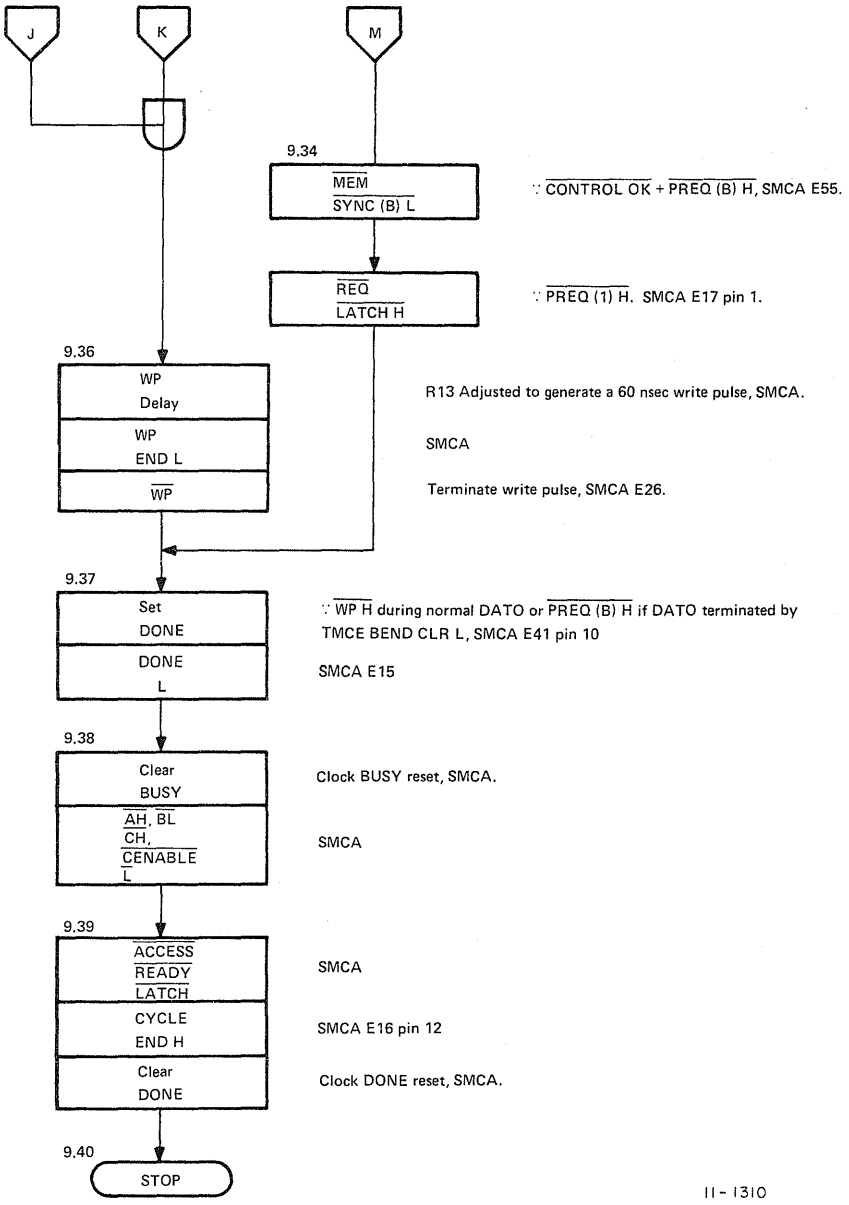


Figure 3-9 Fastbus DATO Logic Flow (Sheet 7 of 7)

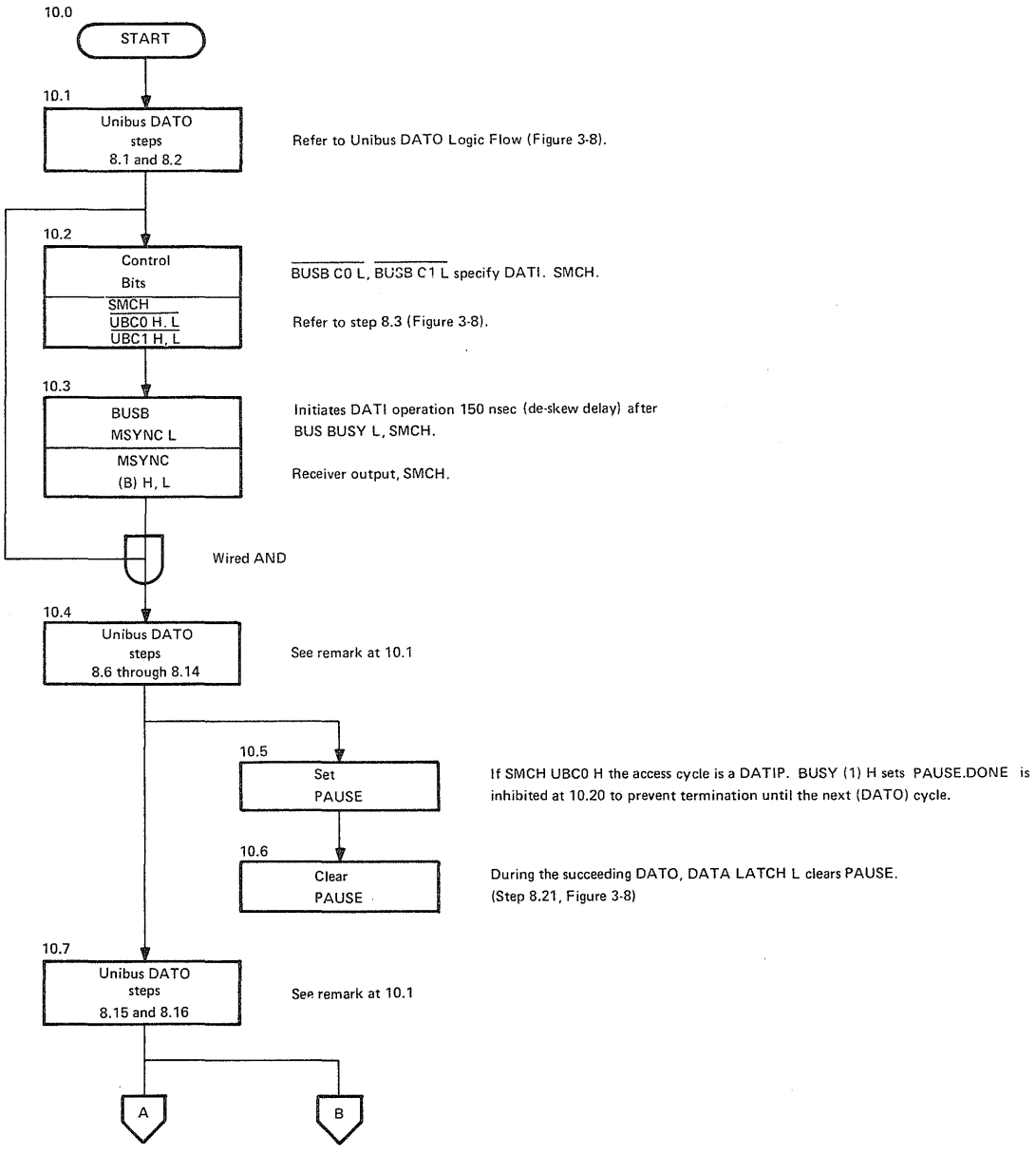


Figure 3-10 Unibus DATI Logic Flow (Sheet 1 of 3)

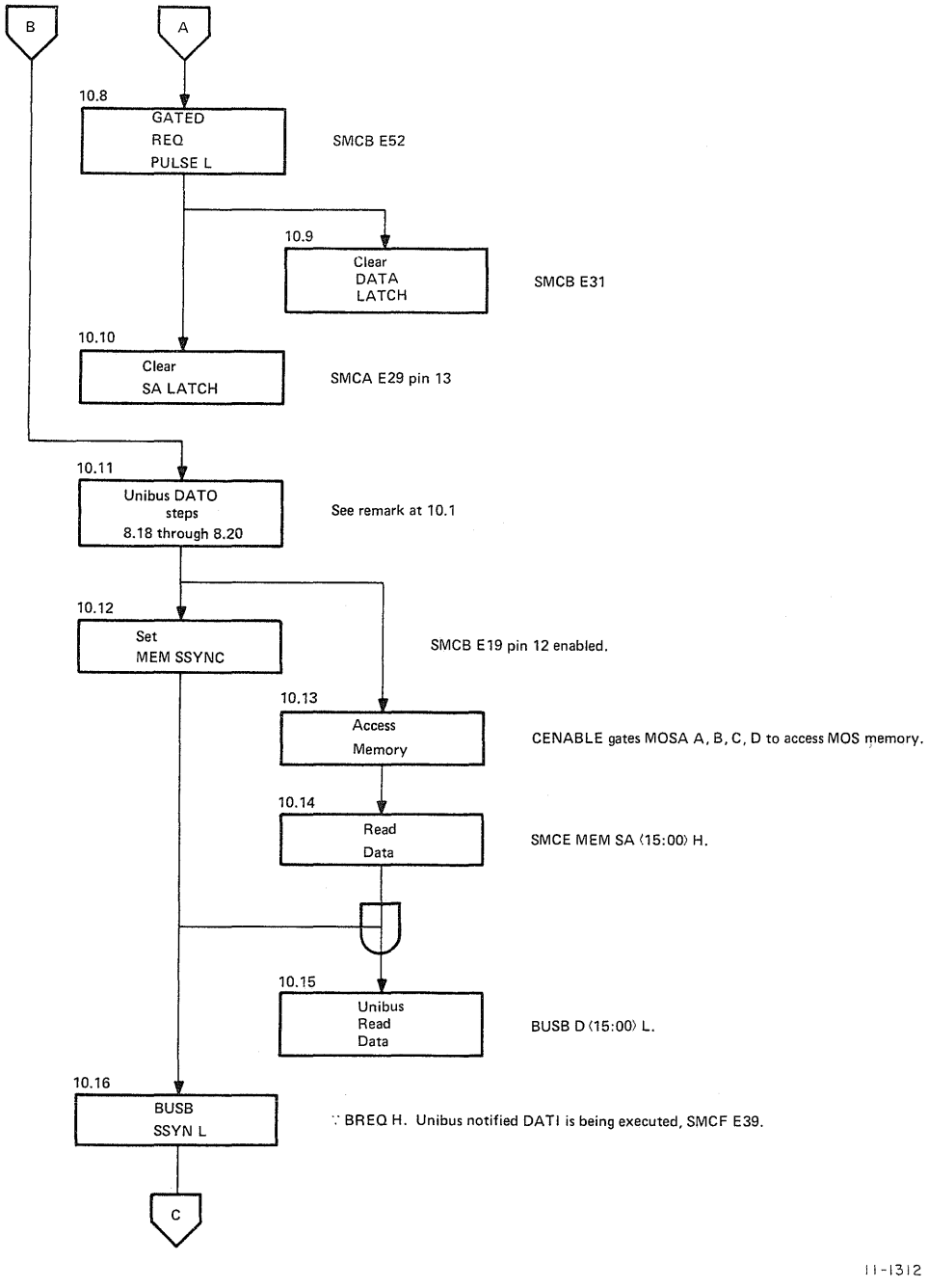


Figure 3-10 Unibus DATI Logic Flow (Sheet 2 of 3)

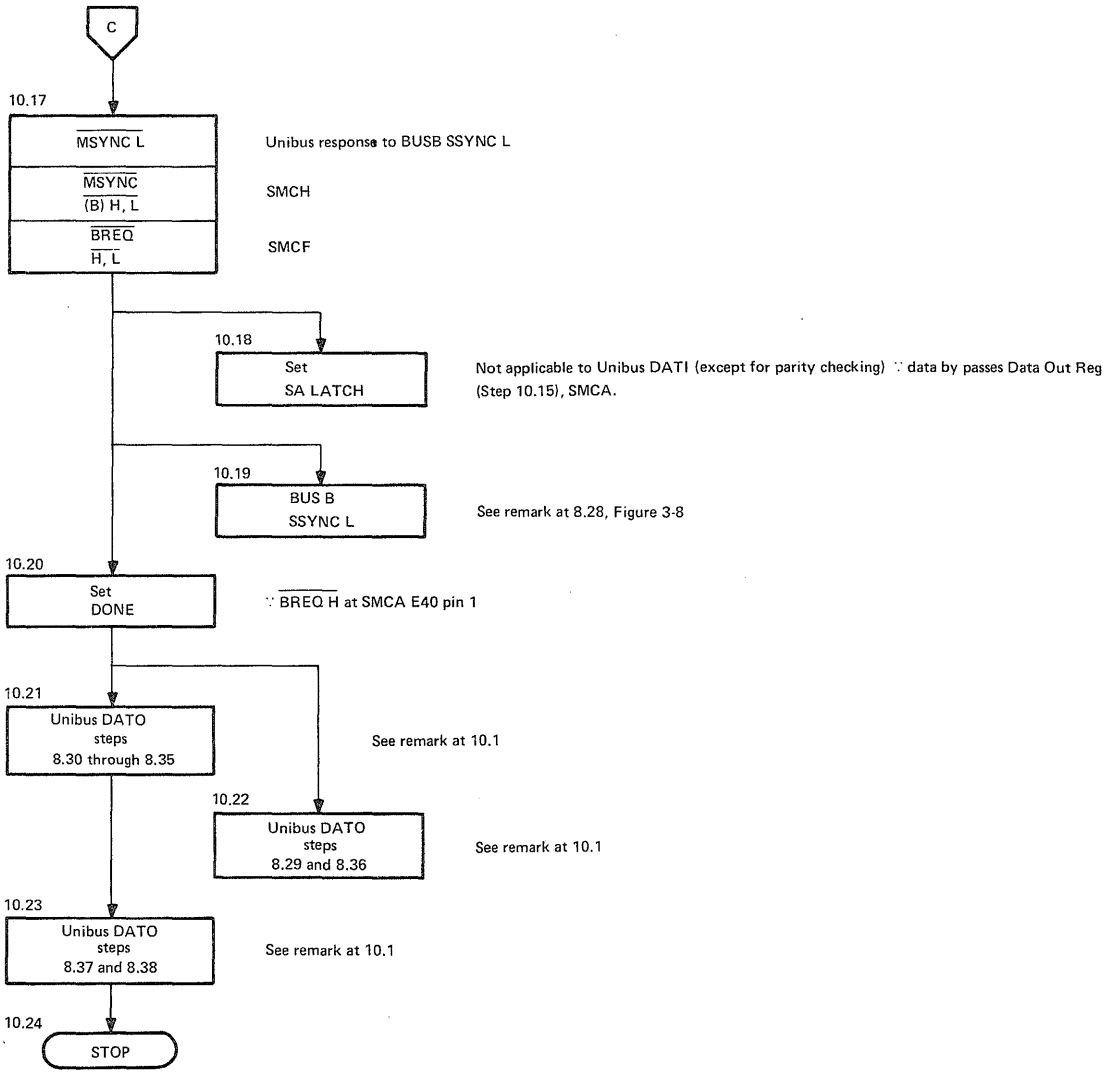


Figure 3-10 Unibus DATI Logic Flow (Sheet 3 of 3)

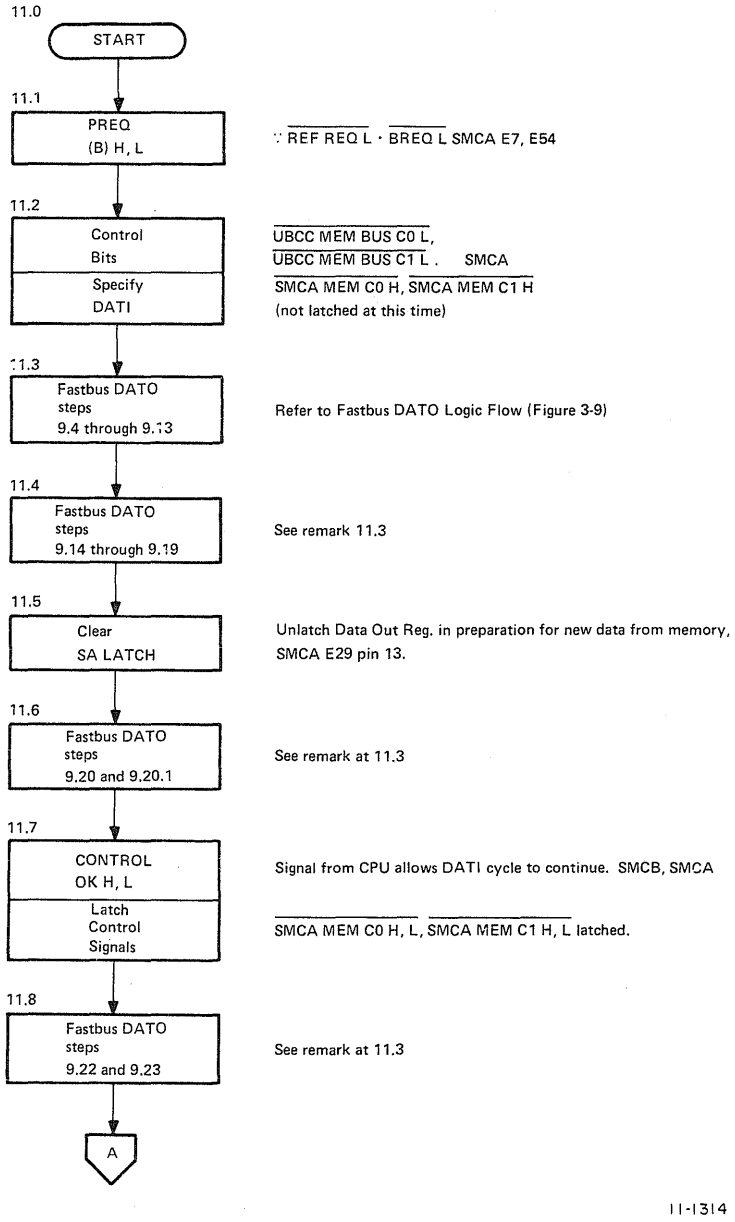


Figure 3-11 Fastbus DATI Logic Flow (Sheet 1 of 2)

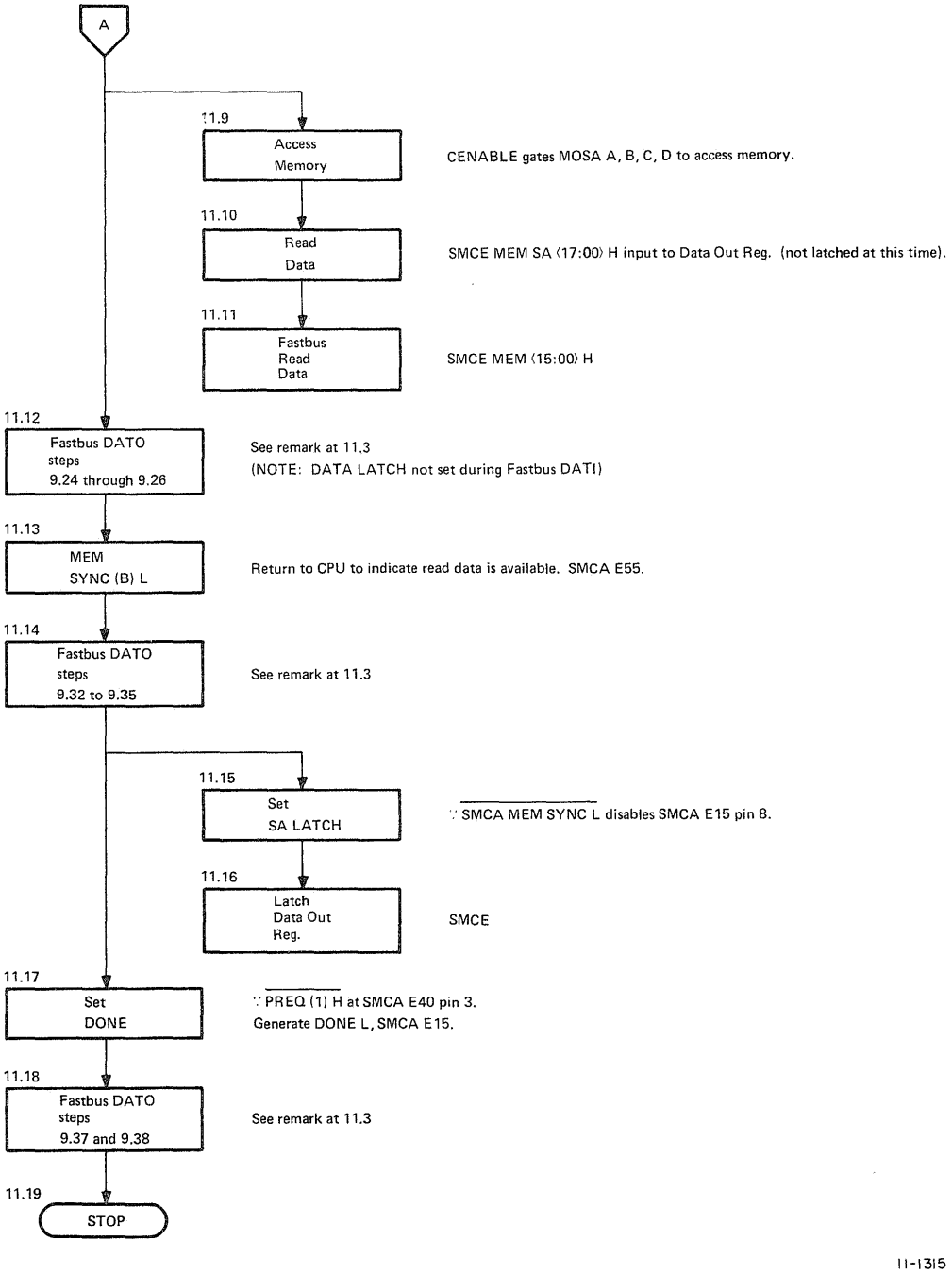


Figure 3-11 Fastbus DATI Logic Flow (Sheet 2 of 2)

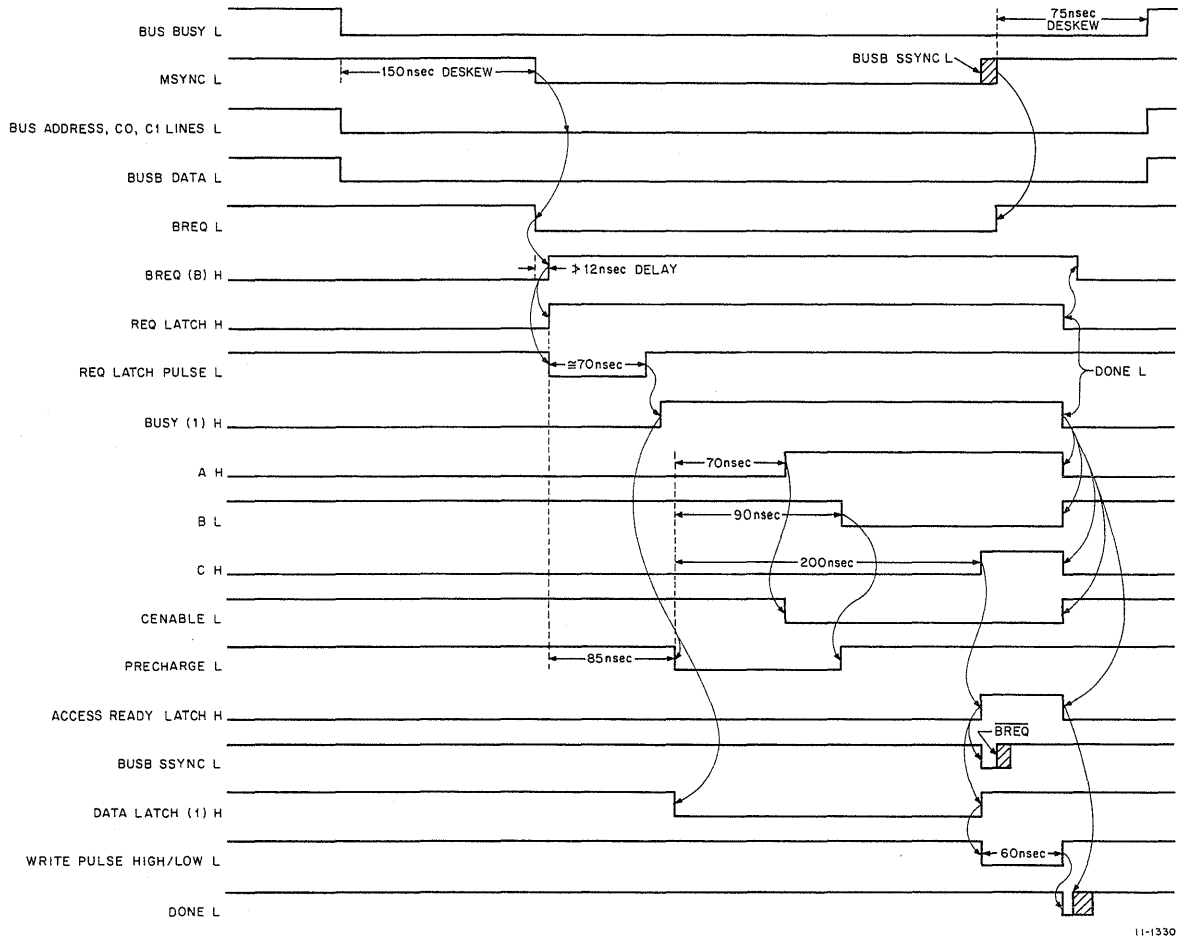


Figure 3-12 Unibus DATO Timing (MOS Memory)

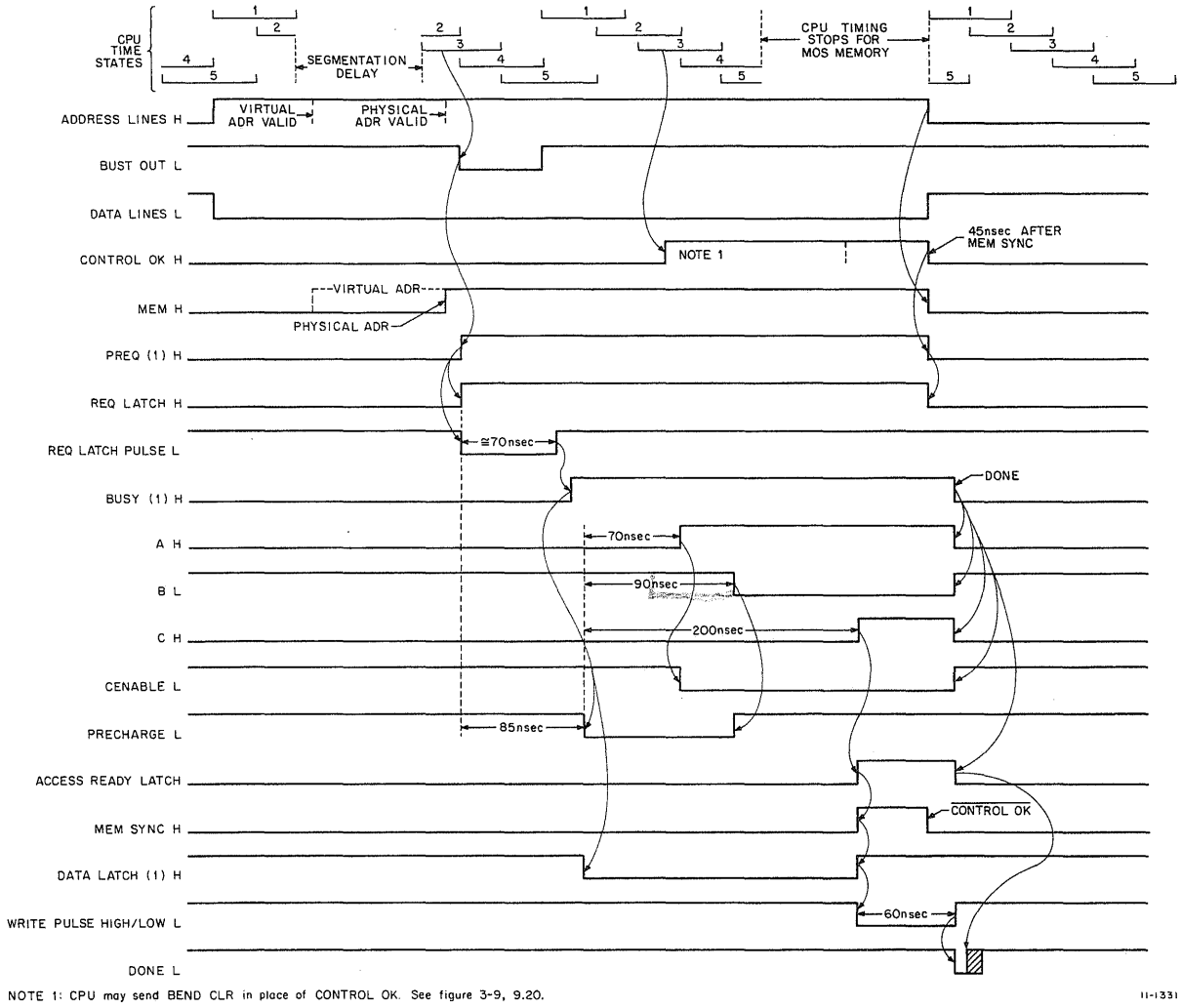


Figure 3-13 Fastbus DATO Timing (MOS Memory)

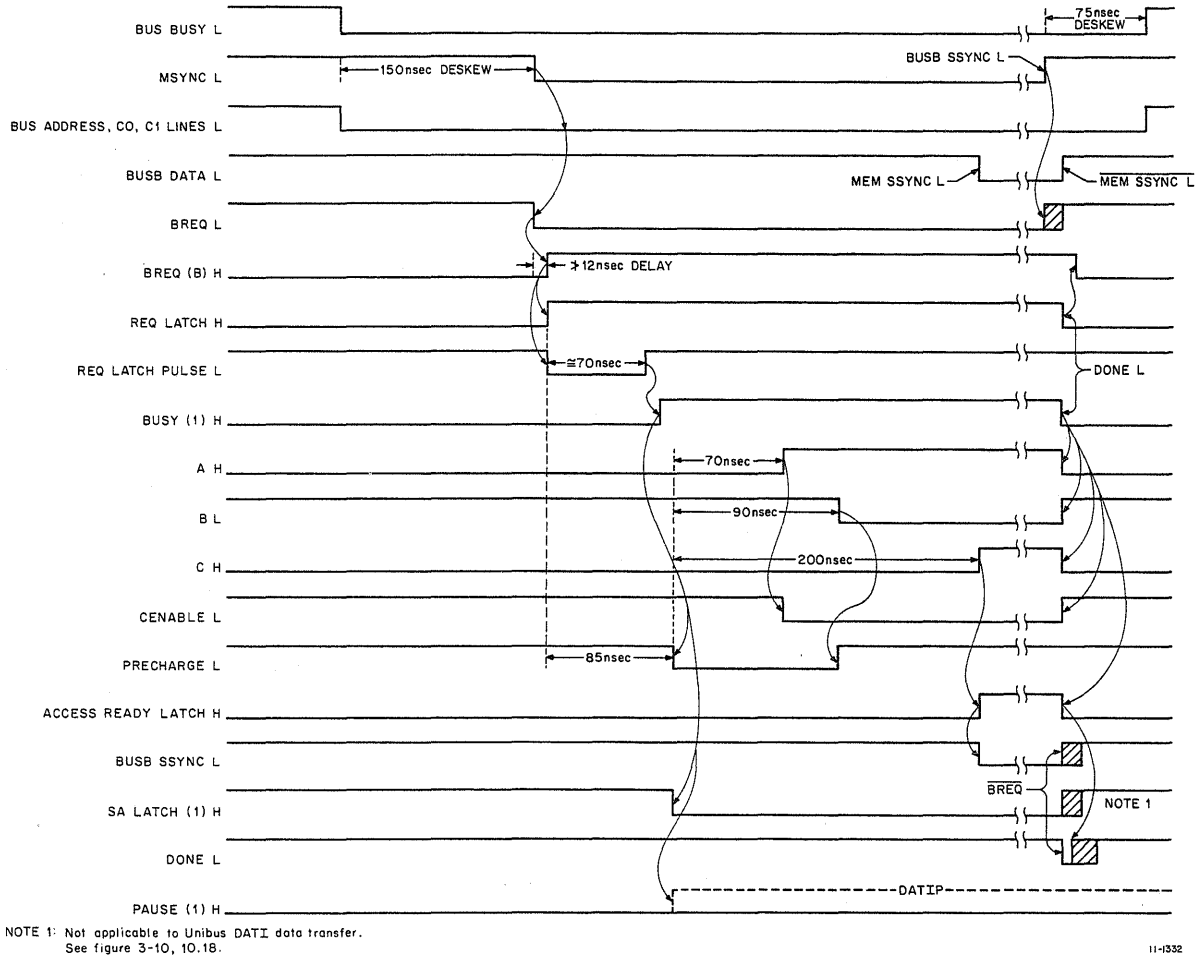
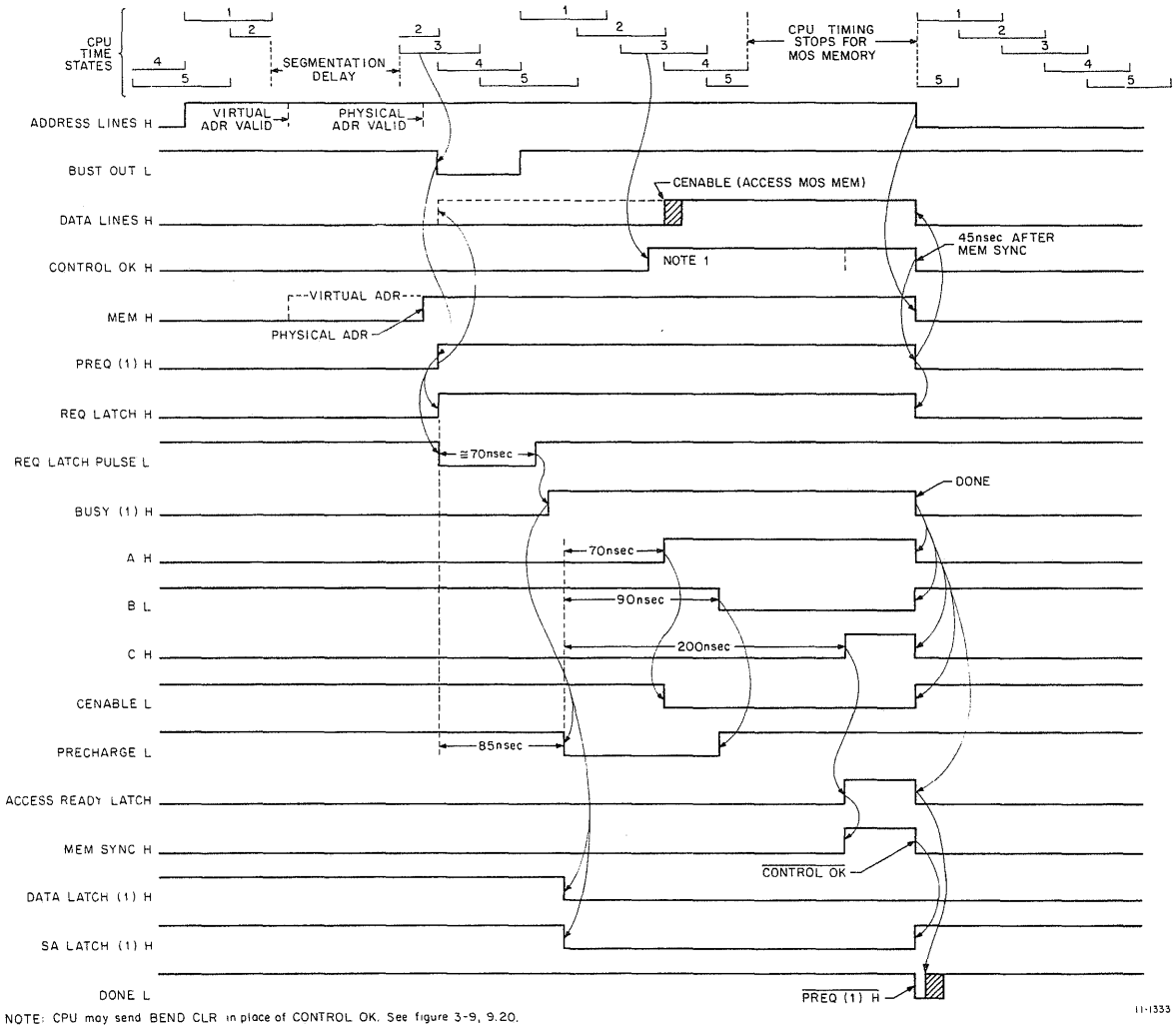


Figure 3-14 Unibus DATI Timing (MOS Memory)



NOTE: CPU may send BEND CLR in place of CONTROL OK. See figure 3-9, 9.20.

Figure 3-15 Fastbus DATI Timing (MOS Memory)

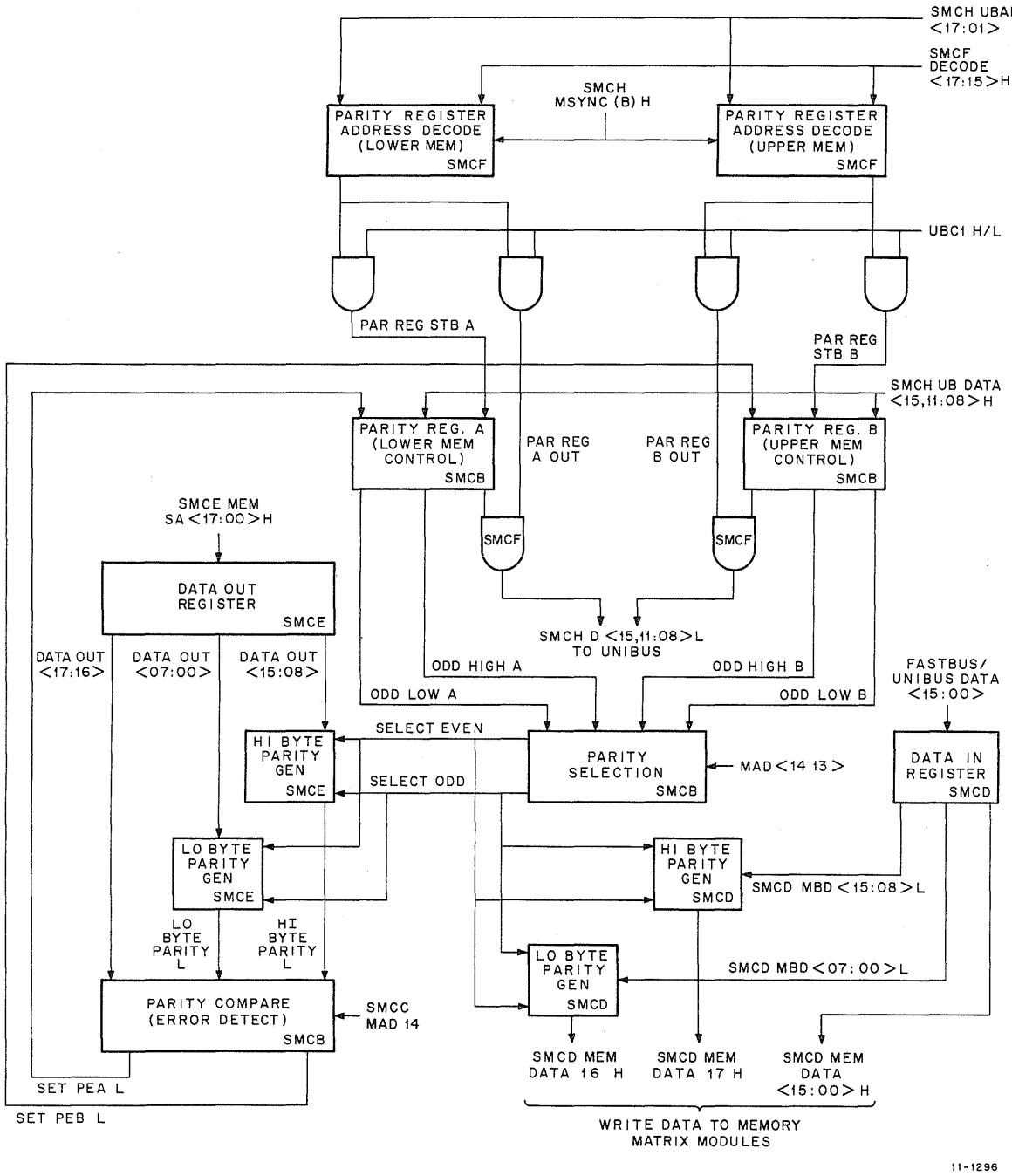


Figure 3-16 Diagnostic Logic Parity Checking and Control

3.4.7.1 **Diagnostic Address Decoding** – In a PDP-11/45 System with a semiconductor memory system, the 18-bit addresses for the four diagnostic parity registers (two per control) would be the octal arrays 772100, 772102, 772104, and 772106 (provided 32K of semiconductor memory is available and started at address 000000_8 and run consecutively to address 177776_8). The address decoding logic at one control is then jumper-wired to decode the first two addresses, and the second control is jumper-wired to decode the second two addresses (drawing SMCF). As a result, the diagnostic parity register address decoding logic at each control consists of two parallel and virtually identical decoding networks. Both networks are conditioned by a third gating structure enabled by the most significant 12 bits, SMCH UBAD ⟨17:06⟩ which decode 7721XX of the diagnostic parity register address. The decoding network consisting of the four exclusive-NOR gates (E95) decodes address XXXX00 (jumper E cut = SMCF DECODE 15 H) or XXXX04 (jumper E in place = SMCF DECODE 15 H), while the decoder consisting of the four exclusive-NOR gates (E94) decodes address XXXX02 (jumper E cut) or XXXX06 (jumper E in place). The four outputs from the NOR gates of each decoder are wire-ANDed to provide a single input to one of the four-input NAND gates, E84. The remaining three inputs to these gates are conditioned in common by SMCH MSYN (B) H, SMCF UBAD 05 L, and the decoding of the most significant 12 bits of the diagnostic parity register address.

Diagnostic register address bits SMCH UBAD ⟨04:02⟩ H are compared with internal levels SMCF DECODE ⟨17:15⟩ H (which are jumper-connected to identify the specific M8110 control) at both exclusive-NOR networks. However, SMCH UBAD 01 H is compared with +3V (logic 1) to designate the upper half of memory under direction of the addressed control, and with ground (logic 0) to address the associated lower half.

The state of SMCH UBC1 (which corresponds to control bit C1 from the Unibus) then determines whether the addressed diagnostic parity register will be written into or read from during the current access cycle.

Either jumper T or jumper B, located at E87, terminal 1, must be cut prior to using the M8110 control. Jumper B is cut when parity control and checking is not desired; jumper T is cut for those configurations that include the parity option.

To summarize the operation of the diagnostic parity register address decoding logic, the state of UBAD ⟨05:01⟩ in such an address, when conditioned by SMCH MSYNC (B) H (which designates a Unibus/semiconductor memory access cycle) and SMCH UBC1, will assert control of the diagnostic parity registers as listed in Table 3-11.

3.4.7.2 **Diagnostic Parity Registers** – Each M8110 control includes two 5-stage registers formed by D flip-flops (drawing SMCB). The common inputs to registers designated REGISTER A and REGISTER B are SMCH UB DATA 15 H and SMCH UB DATA ⟨11:08⟩ H. The inputs and functions of these registers are summarized in Table 3-12.

Parity diagnostic register A controls parity generation and checking in the lower half of memory; register B controls these functions in the upper half of memory. Consider that at control A (lower half of memory) the decoding of the address for parity diagnostic register A is enabled by Unibus assertion of SMCH MSYN (B) H. Because this data is to be written into register A, SMCH UBC1 L will be asserted and SMCF PAR REG STB A H will be asserted at SMCB to clock the data on SMCH UBAD 15 H and SMCH UBAD ⟨11:08⟩ H into register A. Note that at the same control, this data is loaded into register B by PAR REG STB B H, when a register B address is decoded.

Table 3-11
Diagnostic Parity Register A and B Control States

Octal Address	M8110 Control Specified	SMCH UBC1	Parity Register Control Level Asserted	Operation Performed
772100	A	0	PAR REQ A OUT H	Read from register A
		1	PAR REG STB A H	Write into register A
772102	A	0	PAR REG B OUT H	Read from register B
		1	PAR REG STB B H	Write into register B
772104	B	0	PAR REG A OUT H	Read from register A
		1	PAR REG STB A H	Write into register A
772106	B	0	PAR REG B OUT H	Read from register B
		1	PAR REG STB A H	Write into register B

Table 3-12
Parity Diagnostic Register Bit Identity and Function

Input Data	Storage Flip-Flop Name		Parity/Diagnostic Function Performed
	Register A	Register B	
UB DATA 15 H	PEA-parity error register A	PEB-parity error register B	Enables parity error indication to processor when set.
UB DATA 11 H	ODD HIGH A	ODD HIGH B	Odd parity checked in upper 4K when set, even parity when reset.
UB DATA 10 H	ODD LOW A	ODD LOW B	Odd parity checked in lower 4K when set, even parity when reset.
UB DATA 09 H	EHA-halt on parity error register A	EHB-halt on parity error register B	Enables processor halt on parity when set, enables time out trap when reset.
UB DATA 08 H	PIDA-parity interrupt disabled register A	PIDB-parity interrupt disabled register B	Disables all parity-initiated interrupts when set, interrupts enabled when reset.

If register A at control A is to be read, SMCH UBC1 H will be false (C1 = logic 0) so that the decoding of the address for register A will result in asserting SMCF PAR REG A OUT H, which asserts a common enabling line to a set of five NAND gates, E57 and E56 (drawing SMCF). When SMCF PAR REG A OUT H is asserted, the state of each flip-flop in register A, PEA (1) H, ODD HIGH A (1) H, ODD LOW A (1) H, EHA (1) H, and PIDA (1) H is gated onto SMCH D15, D11, D10, D9, and D8 (drawing SMCF). At SMCH, these lines connect directly to the Unibus so that SMCF PAR REG A OUT H, when asserted, transfers the contents of parity diagnostic register A at the addressed control to the Unibus. The level SMCF PAR REG B OUT H performs the same function for register B.

3.4.7.3 **Diagnostic Parity Register Functions** – The following paragraphs present a description of various diagnostic register actions in terms of the logic events implemented by specific flip-flop states and the resulting functions performed. This description is based on the setting and/or resetting of flip-flops in register A and the effects

on the lower 8K section of semiconductor memory. The logic interpretation of register B action and flip-flop states, along with the effects on the upper 8K of semiconductor memory, are exactly the same.

Software can designate the mode of parity generation and the mode of parity checking without correspondence between the two actions. As a result, parity can be generated and checked as odd or even, or generated as odd and checked as even, and vice versa, so that parity error is expected. These parity generation/checking combinations can be applied to a specific 4K section of memory with the remaining memory being unaffected by the parity exercise. This feature provides a powerful tool for diagnosing a memory malfunction and isolating that malfunction to a specific memory word or byte.

By initiating a DATO from the Unibus, one of the two parity diagnostic registers in a given control can be addressed and written into. On this basis, a logic 1 on BUSB D 11 L asserts SMCH UB DATA 11 H at the D input to the ODD HIGH A flip-flop (drawing SMCB).

When register A is clocked by SMCF PAR REG STB A H, SMCA ODD HIGH A (1) H is true. During each subsequent Unibus or Fastbus access cycle, ODD HIGH A (1) H is ANDed with SMCC MAD 13 (1) H and SMCC MAD 14 (0) H. Because SMCC MAD 13 (1) H and MAD 14 (0) H address only one 4K section of the total memory locations under a single M8110 control, odd parity is enabled only for that memory section. ODD LOW A (1) H, ODD HIGH B (1) H, and ODD LOW B (1) H are also ANDed with pertinent states of MAD 13 and MAD 14 to assert parity selectively at the remaining 4K sections of memory. If the input to any of those flip-flops (ODD HIGH A, ODD LOW A, ODD HIGH B, or ODD LOW B) is logic 0, even parity is designated for the selected section of memory (Refer to Tables 3-7 and 3-10 for the relationship of MAD 13 and MAD 14 to memory addressing).

Output from the gating of SMCA ODD HIGH A (1) H, MAD 13 (1) H, and MAD 14 (0) H is ORed with the parity designations for the other 4K memory sections to assert SMCB SELECT ODD H. This level forces odd parity generation if the current access cycle is a DATO, or odd parity checking if the current access cycle is a DATI. If SMCB SELECT EVEN H is asserted, even parity is generated or checked at the 4K memory section designated by the state of the current access cycle address bits MAD 13 and MAD 14.

Each word or byte read from any semiconductor memory matrix module, as a result of either a Unibus or Fastbus DATI, is tested for parity error. If odd parity is generated when a word or byte is written and remains selected when that word or byte is read, then odd parity will be checked. However, the diagnostic program has the option of changing the mode of parity generation and checking for any given set of data. When a word is written during a DATO, bits 16 and 17 are generated as parity bits at SMCD and stored with the word for the high-order (bit 17) and low-order (bit 16) bytes comprising that word. If the access cycle is a DATOB, either bit 16 or 17 will be generated and stored.

When a word is read during a DATI cycle, the complete word is checked for either odd or even parity, depending on whether SMCB SELECT EVEN H or SMCB SELECT ODD H is asserted. On the basis of this check at SMCE, SMCE LOW BYTE PARITY and SMCE HIGH BYTE PARITY are generated, with the state of these levels reflecting the parity of the word currently being read in the mode currently selected. SMCE LOW BYTE PARITY and SMCE HIGH BYTE PARITY are compared with SMCE DATA OUT 16 and 17, respectively, from the current data word by a compare circuit consisting of two exclusive-NOR gates, E71, on SMCB. If a comparison does not occur, indicating that a parity error has been detected, the output from the two exclusive-NOR gates will be low. This low is then inverted to condition two NAND gates, E82. The gates are also conditioned by MAD 14 (1) L and MAD 14 (1) H; these address inputs directed the read to the upper or lower half of memory. On completion of the current DATI, DONE L supplies the final input to the gates. (In addition, SMCA SA LATCH must be set and SMCA BCY must be clear to allow a high at pins 2 and 3 of E82 (SMCB).) If the address of the word read by the current DATI was in the lower 8K, SMCB SET PEA L is asserted. If the address was in the upper 8K, SMCB SET PEB L is asserted. The level asserted sets a corresponding flip-flop (PEA or PEB) in one of

the two parity diagnostic registers. Therefore, for each word read from a semiconductor memory address with an accompanying indication of parity error, a parity error flip-flop in either parity diagnostic register A or B will be set to signal the occurrence of parity error in the associated half of memory.

The diagnostic program has three available options with respect to specifying processor action relative to a parity error (Table 3-12):

a. ignore parity error detection
b. enable processor halt on parity error detection
c. enable processor interrupt on parity error detection

Setting the PIDA or PIDB flip-flop (UB DATA 08 = 1) will result in all parity errors being ignored in the associated half of memory selected.

Detection of parity error during a read cycle sets the PEA flip-flop. If the PIDA flip-flop is reset, SMCB PIDA (0) H and SMCB PEA (1) H assert SMCB PERF L to the processor.

As a result of interrupt handling, the processor asserts UBCB PERF ACKN L to set the PIDA flip-flop. This disables further processor notification of parity error by the associated memory control.

3.4.8 Refresh Logic

The M8110 control contains refresh logic that charges each MOS memory cell above the threshold of the data stored there once every millisecond. This logic is enabled only when the M8110 is controlling G401 memory modules.

A refresh cycle can occur under three different sets of operational conditions:

a. Refresh cycle during normal access operation
b. Refresh cycle intervention during processor single-step instruction mode
c. Refresh cycle during power-down periods

Each of these conditions is described separately in the following paragraphs.

3.4.8.1 Normal Refresh Cycle – A normal refresh cycle (Figure 3-17) consists of simultaneously addressing one of 32 rows at each G401 MOS Memory Matrix module (drawing SMCB). Each row addressing cycle is timed by a 30-μs free running clock. This clock is formed by the RC network C140 and R66, which is base-collector coupled to the NPN switching transistor Q1. The emitter of Q1 is coupled through three inverter stages and fed back to the base of Q1. The 30-μs square-wave output of the clock, SMCB REF CLOCK H, is taken off the output from the first inverter stage as a 30-μs square wave. SMCB REF CLOCK H is a continuous clocking input to the REF REQ flip-flop. The D input to this flip-flop is +3V; therefore, when clocked, the output of this flip-flop is REF REQ (1) H, which is gated with BIPOLAR L to assert REF REQ L.

NOTE

Jumper A (SMCB) must be cut for MOS memories. Therefore, BIPOLAR L is always high for MOS memories and always low for bipolar memories. The purpose of this level is to disable the refresh cycle when the M8110 control is directing an M8111 Bipolar Memory Matrix module.

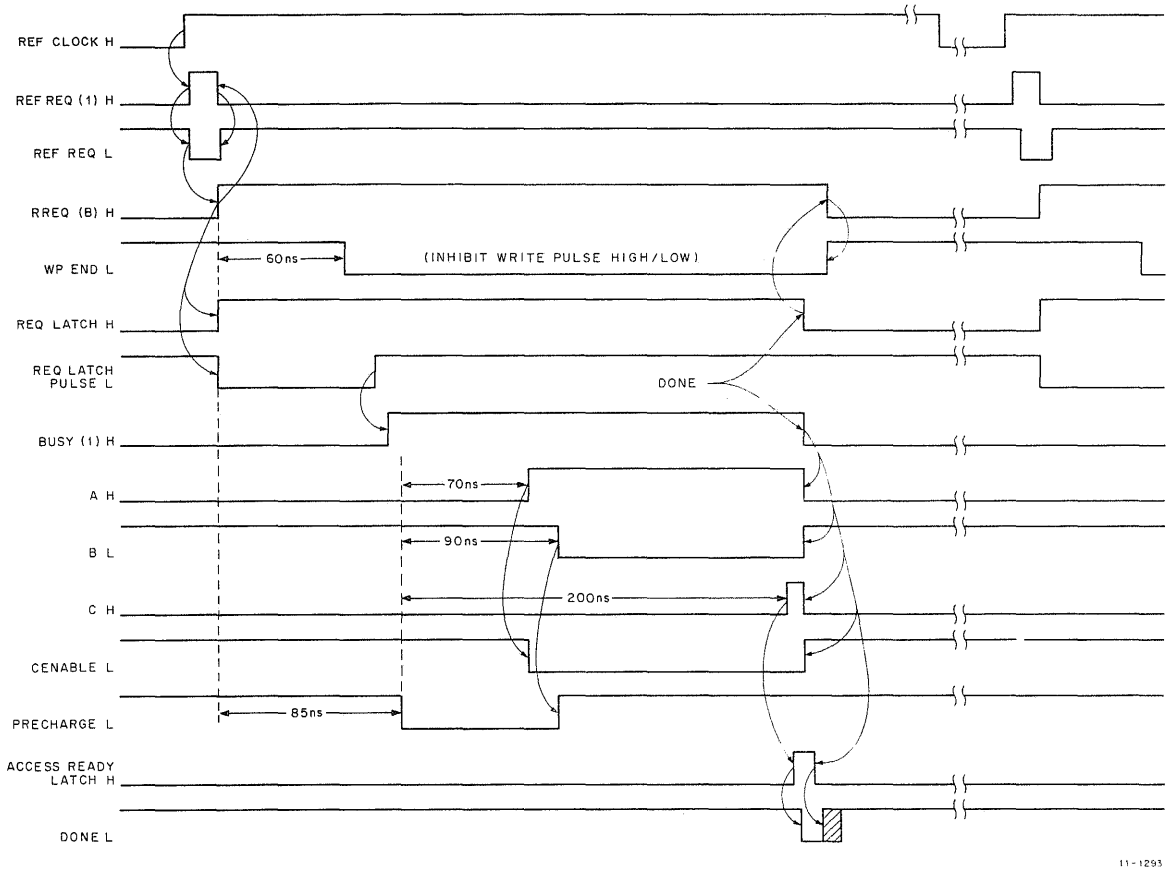


Figure 3-17 Normal MOS Refresh Cycle Timing

REF REQ L is input to a latch (E51) which asserts SMCA RREQ (B) H (drawing SMCA). SMCA RREQ (B) H initiates an access cycle in the same manner as the Unibus or Fastbus, resulting in the assertion of SMCA REQ LATCH PULSE L. SMCA REQ LATCH PULSE H is ANDed (SMCA) with SMCA RREQ (B) H to generate SMCA RREQ ADDR EN L. This pulse multiplexes the current refresh address SMCB RFAD ⟨04:00⟩ H onto SMCC MAD ⟨07:03⟩ to the memory plane (Table 3-10). Note that if an access cycle from the Unibus or Fastbus is underway, coincident with one of the synchronous assertions of RREQ L, all subsequent assertions of PREQ L will be locked out until the current access cycle is complete. This lock-out action is effected by SMCA REQ LATCH H, which is asserted during all access cycles. SMCA REQ LATCH inhibits the output of the latching element responsible (E51, pin 4) for assertion of SMCA RREQ (B) L, SMCA RREQ (B) H, and SMCA RREQ IN PROG L.

When RREQ (B) L is generated, a 60-ns delay is initiated at the termination of which SMCA WP END L is produced at SMCA E14, pin 9. This signal will inhibit any write pulse from NAND gates E26 (SMCA) when ACCESS READY LATCH H is asserted at the end of the timing cycle. The REF REQ flip-flop is cleared (SMCA E127, pin 13) as the result of its own outputs. REF REQ L (derived from REF REQ (1) H) raises RREQ (B) H which, in turn, generates SMCA REQ LATCH PULSE H via SMCA E17, pin 9. This latter signal is ANDed (SMCB E128, pin 3) with RREQ (B) H to clear the REF REQ flip-flop; REF REQ L is inhibited until the next REF CLOCK signal.

The refresh address is output from a 5-stage binary counter, formed by a 4-bit synchronous binary counter (E129) and a D flip-flop (E130), which forms the fifth and most significant stage. This 5-stage counter, shown on drawing SMCB, is clocked by REF CLOCK H.

SMCA RREQ IN PROG L forces the memory gating control levels (MOSA A, B, C, and D) simultaneously high at each 3207 TTL/MOS level shifting gate, so that as G401 module CENABLE and PRECHARGE are asserted, these levels are gated to every 1103 MSI memory circuit comprising each G401. In addition, the current 5-bit row address SMCC MAD ⟨07:03⟩ (1) H is gated into the two address inputs to all G401 MOS memory modules at the same time. Therefore, with the coincidence of a given row address, SMCA CENABLE L, and SMCA PRECHARGE L, 32 corresponding data words are refreshed simultaneously in each 1024-word section of the four G401 MOS memory modules for a total of 128 words per refresh cycle. When SMCA ACCESS READY LATCH H is asserted in the refresh cycle, SMCA DONE L is asserted and the cycle is complete. The next refresh cycle will not start until the next positive-going transition of SMCB REF CLOCK H.

3.4.8.2 **Refresh Cycle Intervention During Single-Step Mode** – During the single-step execution of processor instructions resulting in a DATO or DATI from either the Unibus or Fastbus, it is possible that a given access cycle could encompass two or more processor microstate (or machine) cycles. In such cases, the access cycle can be initiated from the Unibus or Fastbus during one cycle, with address and data being propagated to the addressed M8110 control on the next cycle. Because execution time of this next cycle in the single-step mode is dependent upon human response, long time periods could elapse between two such cycles. In order to maintain validity during these periods, the refresh logic is structured to permit intervention in single-step-initiated access cycles in order to refresh data. This intervention has no effect on the current access cycle.

In the normal refresh cycle, the REF REQ flip-flop is clocked on the positive-going edge of SMCB REF CLOCK H to assert SMCB REF REQ (1) L and, thereby, start a refresh cycle. However, if after memory is selected there is a single-step (mode) initiation of a Unibus or Fastbus access cycle, SMCA ACCESS READY LATCH will remain high for longer than normal if the access cycle is split between two processor cycles. Consequently, DONE L is asserted for an inordinately long period, inhibiting the normal refresh cycle (Paragraph 3.4.8.1) at SMCA E17, pin 10. This characteristic of a memory access cycle in the single-step mode is detected at a logic circuit shown on drawing SMCB. This structure is an integrating one-shot multivibrator formed by one element of a 75107 line receiver (E125), combined with an external RC made up of discrete resistors R101, R102, R103, and capacitor C139. The period of this one-shot is 15 μs. When SMCB REF REQ L is asserted, this one-shot is triggered so that 15-μs later, if conditioned by SMCA ACCESS READY LATCH H, SMCB REF TIME OUT L becomes true. The effect of asserting this level is as follows: when a refresh cycle is requested but not successfully completed within 15 μs after SMCB REF REQ L becomes true, the logic sequence for initiating a refresh cycle, irrespective of memory state, is enabled. When asserted, SMCB REF TIME OUT L activates the termination logic at SMCA E15 and SMCA DONE L is asserted. SMCA DONE L then unlatches the 74S64 logic (E17) enabled by the current single-step mode access cycle and forces SMCA REQ LATCH false. With SMCA REQ LATCH false, SMCB REF REQ L can change the state of the 3404 latching element at SMCA E51 to assert SMCA RREQ (B) H, thereby enabling SMCA E17 and restarting a refresh cycle.

Because activity in the single-step mode is based on a human, rather than machine, time reference, the state of an access cycle is, for all practical effect, frozen. As a consequence, the approximately 450-ns refresh cycle is performed on a cycle-steal basis with respect to the current access cycle. All control levels pertinent to the current single-step mode access cycle remain asserted, so that upon completion of the subject refresh cycle, the addressed M8110 reverts to the state specified by that access cycle. In addition, completing the subject refresh cycle results in resetting the REF REQ flip-flop and disabling SMCB REQ L. At this point, the 15-μs delay is terminated.

3.4.8.3 **Refresh Cycle During Power-Down Periods** – The free-running clock (SMCB E104) will continue to cycle during power down situations and (30 μs) REF CLOCK H signal production is maintained. Unless PWRS MEM DC LO L is received (SMCH E36), +5V will be present at the collector of Q1 and the clock generator will function as in normal power-up periods. Response of the memory refresh logic to REF CLOCK H is the same as during the normal refresh cycle (Paragraph 3.4.7.1 and Figure 3-17).

CHAPTER 4
CALIBRATION AND MAINTENANCE

4.1 INTRODUCTION

This chapter concerns the calibration procedures and maintenance requirements necessary to maintain an MS11 Semiconductor Memory System. Paragraph 4.3 presents the detailed procedures necessary to perform all memory system adjustment and calibration. The section on maintenance includes lists and descriptions of the diagnostic program set required to perform memory system troubleshooting. Also included are references to specific maintenance requirements contained in associated PDP-11/45 System documentation.

4.2 SEMICONDUCTOR MEMORY SYSTEM PRECALIBRATION PROCEDURES

Certain steps must be taken prior to actual memory calibration in order to assure valid results. These include loading a simple memory cycling program, assembling the correct tools and equipment, and verifying that all portions of the memory system and the overall PDP-11/45 System are operational. These steps are presented in the following paragraphs.

4.2.1 Memory Cycling Program

Proper performance of the adjustments listed in Table 4-1 requires that the semiconductor memory be continuously cycling during actual calibration. While the memory refresh function automatically (during a power-up or power-down condition) provides this requirement for MOS memory configuration, bipolar installations require the input of a simple two-step program to implement continuous memory cycling. This program forces a DATI to the memory system being calibrated every four KB11 bus cycles. Load this program into the processor through the console switches as outlined in the following procedure:

Step	Procedure
1	Set the octal address NNN 200 in the console switch register.
	NOTE **The three leading digits of this address define a core or semiconductor memory area other than the semiconductor memory being calibrated.**
2	Press the console LOAD ADRS switch.
3	Set 13700_8 in the console switch register and press DEP.
4	Place any address from within the semiconductor memory area being calibrated in the console switch register and press DEP.
5.	Set 000775_8 in the console switch register and press DEP.
6.	Repeat Steps 1 and 2, then press START.

Table 4-1
Semiconductor Memory Adjustments

Adjustment	Pin Nos.	Purpose
R42 REQ LATCH PULSE L	E17 pin 8 to E24 pin 8	Delays start of memory access cycle until address lines are stable
R7 AH/CENABLE	E24 pin 8 to E24 pin 6	Times the assertion of AH, which, in turn, asserts CENABLE to enable the memory chips addressed
R9 BL/PRECHARGE	E24 pin 8	Times the assertion of BL, which defines the trailing edge of PRECHARGE to complete recharging of MOS memory prior to accessing
R11 CH ACCESS READY LATCH	E24 pin 8 to E16 pin 12	Times the assertion of CH, which asserts ACCESS READY LATCH to implement the current access cycle.

At this point, a continuous DATI cycle will be performed at the M8110 control to be calibrated. Note that this program originates from a memory area remote from the memory being calibrated so that the test program will be unaffected by the calibration procedure. Upon completion of a calibration procedure, the test program can be terminated by pressing the console HALT switch.

4.2.2 Test Equipment Required

Calibration of M8110 control timing is best performed with a Tektronix 453 oscilloscope or an equivalent equipped with P6000-type probes. Also required for this calibration procedure are three, dual height, DEC W900 multilayer extender boards and two IC chip clips.

4.2.3 Calibration Setup

Before adjusting the semiconductor memory system, perform the following steps:

Step	Procedure
1.	Verify that all semiconductor system modules are properly installed in the correct CPU backplane slots as shown in Drawing E-MU-KB11-A-01 in the *PDP-11/45 System Engineering Drawings.*
2.	Visually check modules for such obvious defects as broken wires and connectors.
3.	Turn on primary power and verify that the overall computer system is operational.

4.3 MEMORY SYSTEM CALIBRATION

The characteristically different operating speeds of MOS and bipolar memory systems, and the resulting difference in timing, requires separate calibration procedures for the system adjustments listed in Table 4-1.

4.3.1 MOS Memory System Calibration

The following procedures delineate all necessary adjustments to an M8110 memory control directing G401 MOS Memory Matrix modules.

4.3.1.1 Address Set Up, Precharge, CENABLE, and Access Ready Timing Adjustments

To perform address set up, precharge, CENABLE, and access ready timing, proceed as follows:

Step	Procedure
1.	Remove the M8110 control from the processor and install the W900 extender boards in its place.
2.	Plug the M8110 control into the W900 extenders.
3.	It is not necessary to load the program described in Paragraph 4.2.1; the refresh logic causes MOS memory to be cycled continuously.
4.	Set the oscilloscope as follows: place SLOPE switch in the minus (-) position; set the SOURCE switch to INT SOURCE; press the INT TRIGGER button on CHANNEL 1 only; set the TIME BASE switch to 20 ns/cm; and set the VOLTS/DIV switch to 0.5V/cm. All time measurements are made from the -1.5V point on the displayed waveforms.
5.	Locate IC 17 and IC 24 on the M8110 module and place an IC chip clip on each device.
6.	Place the oscilloscope A probe on pin 8 of IC E17 (input); place the B probe on pin 8 of IC E24 (output).
7.	Refer to Figure 4-1, which shows the relationship of the oscilloscope A Trace to the B Trace.
8.	Locate R42 on the M8110 module and adjust the delay until the leading edge of B Trace occurs approximately 85 ns after the leading edge of A Trace. **NOTE** **The size of the slotted-head adjusting screw on R42 requires a small screwdriver with a thin blade. Such a tool can be made by grinding or filing the blade of a 3-in. pocket-type screwdriver until it fits the delay-adjusting screw.**
9.	Remove the oscilloscope probes; attach the A probe to pin 8 of IC E24 and the B probe to pin 6 of IC E24.
10.	Refer to Figure 4-1, then locate and adjust R9 until the A Trace shows a 90-ns negative-going waveform, ±1 ns.
11.	Refer to Figure 4-1, then locate and adjust R7 until the negative-going leading edge of B Trace occurs 70 ns after the negative-going trailing edge of the A Trace.
12.	Remove the IC chip clip from IC E17 and place it on IC E16.
13.	Attach the B probe to pin 12 of IC E16. This is CYCLE END H; it is used to define the access time (ACCESS READY LATCH L).
14.	Refer to Figure 4-1, then locate and adjust R11 until the negative-going leading edge of B Trace occurs 200 ns ±1 ns after the leading edge of A Trace.
15.	Remove the probes and chip clips.
16.	Reinstall the M8110 Semiconductor Memory Control in its original connector slot.

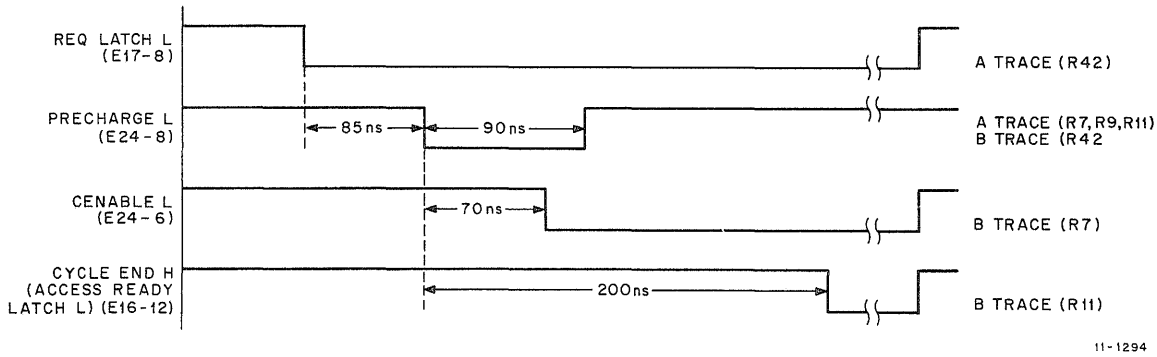


Figure 4-1 M8110 Timing and Termination Delay Adjustment for MOS Memory (Logic Drawing SMCA)

4.3.2 Bipolar Memory System Calibration

The high speed of bipolar memory systems requires that several M8110 control delay adjustments can be calibrated differently than for an MOS memory system. The procedures for these adjustments are exactly the same as the equivalent MOS memory system adjustment, except for the actual duration of the delay. As a consequence, the procedures for bipolar memory system calibration will reference pertinent MOS calibration procedures wherever applicable.

4.3.2.1 Address Set Up, Precharge, and Access Ready Timing Adjustments

To perform address set up, precharge, and access ready timing adjustments, proceed as follows:

Step	Procedure
1.	Repeat Steps 1, 2, 4, 5, and 6 of Paragraph 4.3.1.1. Load the program described in Paragraph 4.2.1.
2.	Refer to Figure 4-2, which shows the relationship of the A Trace to the B Trace.
3.	Repeat Step 8 of Paragraph 4.3.1.1.
4.	Remove the oscilloscope probed; attach the A probe to pin 8 of IC E24.
5.	Refer to Figure 4-2, then locate and adjust R9 until the A Trace shows a 60-ns negative-going waveform, ±1 ns.
6.	Repeat Steps 12 and 13 of Paragraph 4.3.1.1.
7.	Refer to Figure 4-2, then locate and adjust R11 until the negative-going leading edge of B Trace occurs 60 ns ±1 ns after the leading edge of the A Trace.
8.	Repeat Steps 15 and 16 of Paragraph 4.3.1.1.

4.4 SEMICONDUCTOR MEMORY SYSTEM DIAGNOSTICS

The *PDP-11/45 System Maintenance Manual,* Chapter 9, presents a brief abstract for each diagnostic, describing program function and application.

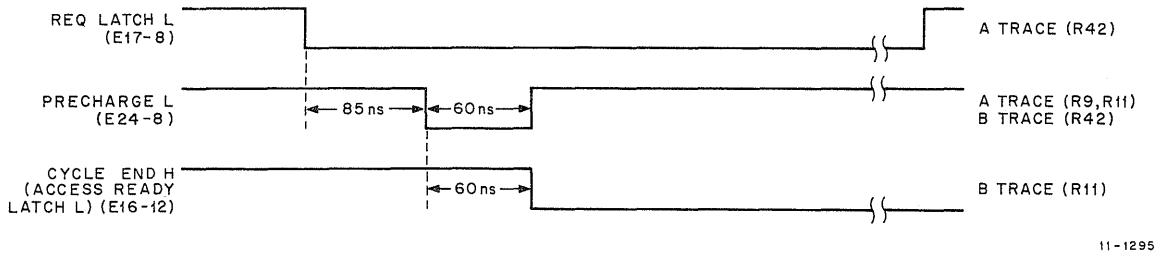


Figure 4-2 M8110 Timing and Termination Delay Adjustment for Bipolar Memory (Logic Drawing SMCA)

4.5 MEMORY MATRIX MODULE STRUCTURE

The relationship of G401 MOS Memory Matrix Module ICs to function is shown in Figure 4-3; Figure 4-4 provides similar information for M8111 Bipolar Memory Matrix Modules.

4.5.1 Isolation of Malfunctions to Module Component

Various means are available to maintenance personnel to identify the source of memory errors: signal tracing using the oscilloscope and other test devices, diagnostic software that exercises selected areas of logic, and replacement of suspected modules with identical spares that are known to be operational. The method (or methods) used is determined by such factors as the nature of the problem, availability of on-line time and test equipment, applicable maintenance directives, and instructions from supervisory (maintenance) personnel.

Isolation of memory problems to the module level involves identifying the failing address(es) and determining which module has been assigned this address. As previously described (Paragraph 3.4.1) the jumper configurations on the M8110 Semiconductor Memory Control(s) and the G401/G401YA and M8111/M8111YA Memory Matrix Modules determine this memory address assignment (refer to Tables 3-1, 3-2, 3-5, 3-7, 3-8, and 3-9). The processor, through software, is able to identify the failing address(es); this is accomplished by such means as the ability to generate and check the parity (odd or even) of data stored in 4K sections of memory and to write 8-bit bytes in addition to 16-bit words. (It should be noted that parity testing operations require the presence of a memory with the parity option.) These selective methods of storage, in conjunction with the processors "error halt" facility, provide a very positive means for processor identification of failing memory address.

Identification of the faulty IC in the memory matrix module is the logical conclusion of this procedure where known data is stored at and read from known locations, with the processor halting when errors are discerned. As indicated in Figures 4-3 and 4-4, 256 or 1K word memory areas (high byte and low byte), storage bits, and control circuits are identifiable to the component (IC) level. (The "E" numbers for these ICs can be found on drawings E-CS-G401-1 (MOS) and E-CS-M8111-0-1 (bipolar)).

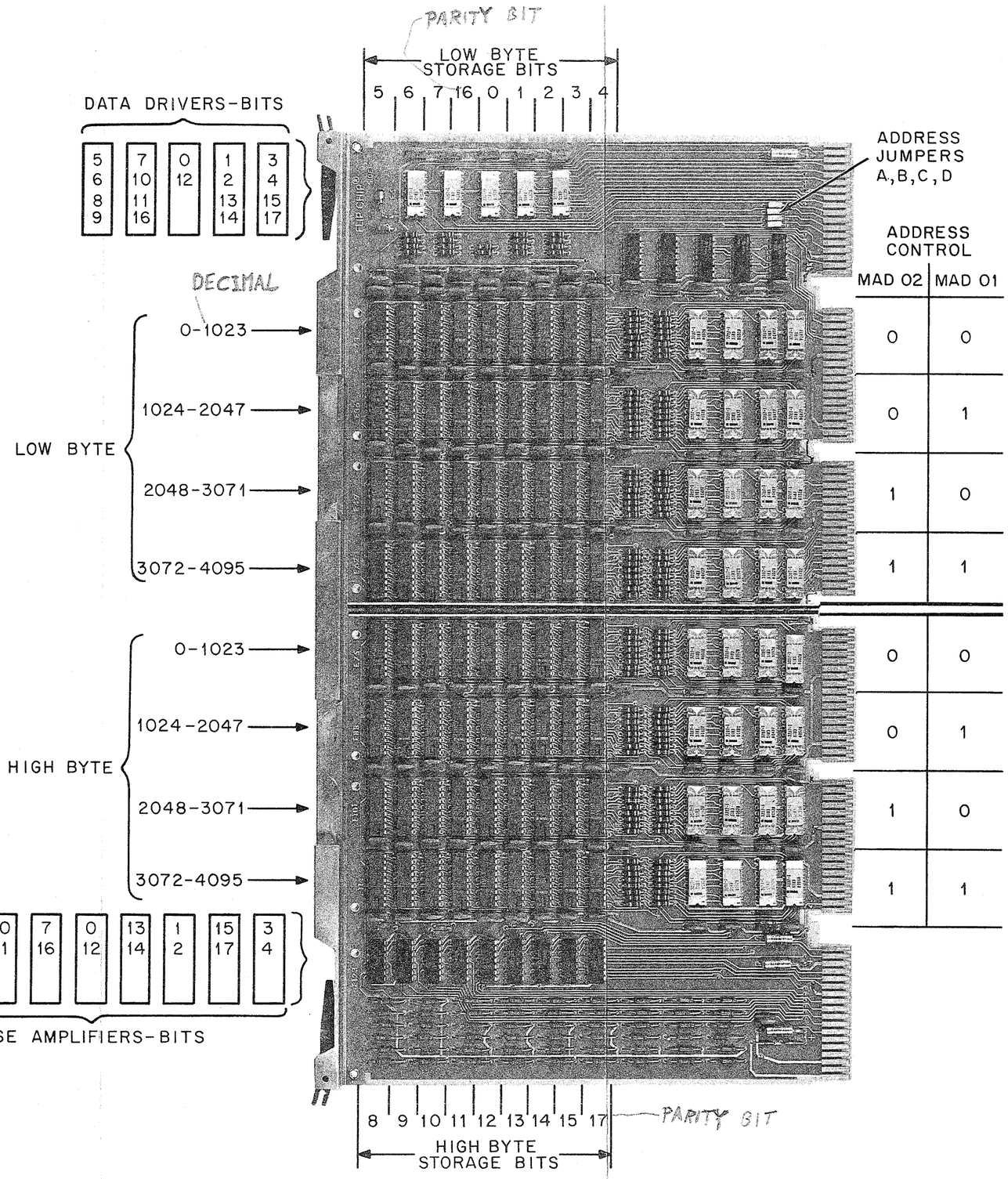


Figure 4-3 G401YA MOS Memory Matrix Module - Relationship of ICs to Bits

ROW SELECTION MAD 09	08	ROW	LOCATIONS	
1	1	3	768-1023	HIGH BYTE LOW BYTE
1	0	2	512-767	HIGH BYTE LOW BYTE
0	1	1	256-511	HIGH BYTE LOW BYTE
0	0	0	0-255	HIGH BYTE LOW BYTE

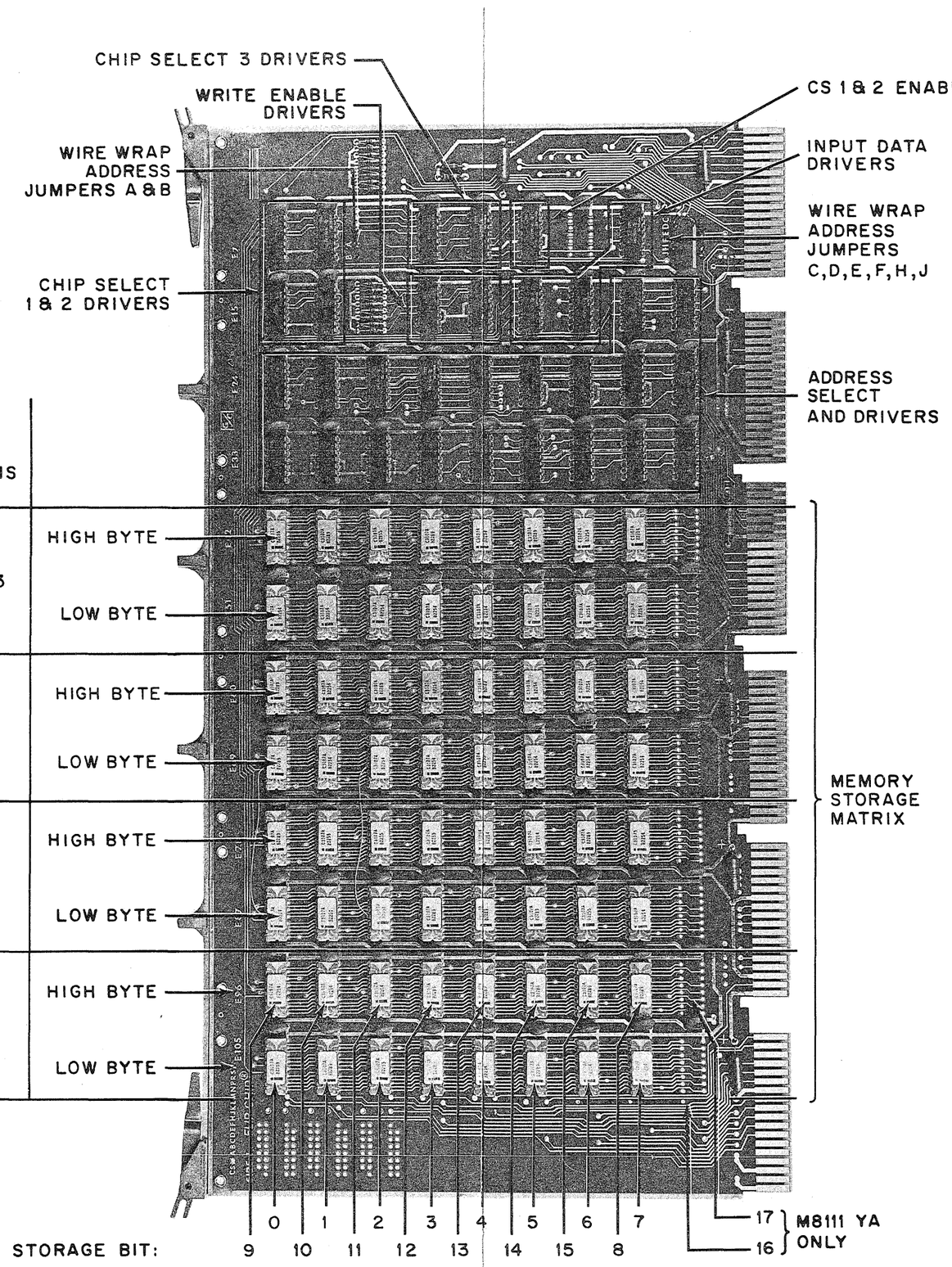


Figure 4-4 M8111 Bipolar Memory Matrix Module - Relationship of ICs to Bits

APPENDIX A
APPLICATION OF MOSFETS IN IC RANDOM ACCESS MEMORIES

A.1 INTRODUCTION

The primary purpose of this discussion is to provide a general insight into the operation and use of the metal-oxide silicon field-effect transistor (MOSFET). A basic understanding of transistor terms and operation is assumed.

The first part of this discussion presents a general description of MOSFET operation, particularly in the role as a switch, a normal transistor application. The second part discusses the use of the MOSFET in memory application and deals specifically with the basic integrated memory cell used on the DEC G401 MOS Memory Matrix module.

A.2 THE MOSFET

The MOSFET is a voltage-controlled semiconductor characterized by small geometries, high input impedance, low power consumption, and simplicity of fabrication (Figure A-1). In addition, the nature of the MOSFET precludes the need for extensive device isolation within an integrated substrate, thereby making the MOSFET an ideal device for medium and large scale integration. The connections to a MOSFET, as shown in Figure A-1, are the source, the drain, and the gate. The operation of a MOSFET is based on an electric field produced in the metal-oxide insulating layer by a voltage at the gate electrode which controls the charge in the semiconductor channel, thereby governing the current in the source-drain path. There is no conducting path between the source and the drain when the gate electrode is an open circuit. However, when the gate is made negative with respect to the source and drain, an electric field is produced in the metal-oxide layer under the gate. This field originates at the positive charge in the semiconductor substrate and terminates in the negative charge in the metal gate electrode. The positive charge consists of holes left in the semiconductor substrate in the region under the gate electrode. The resulting charge is mobile, thereby completing a conductive path, or P channel, between the source and the drain.

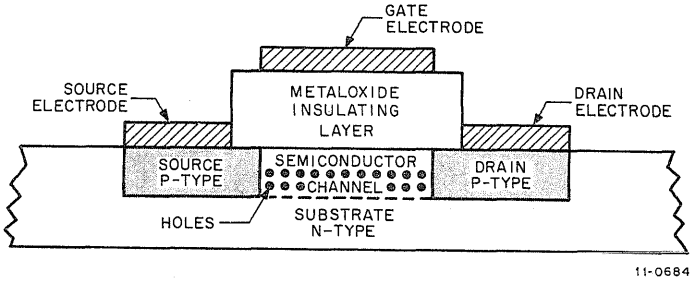


Figure A-1 Physical Structure of a MOSFET
(physical relationships are exaggerated for clarity)

The conductors of the channel induced by the gate depend on the gate-to-source voltage. This dependence is demonstrated by plotting the drain current against the drain-to-source voltage with voltage gate-to-source as a parameter. Since, as demonstrated in Figure A-2, little or no current is required in the gate circuit because of insulation provided by the metal-oxide layers, only a small amount of power is necessary to contact the power in a loop compressing the source-to-drain path. On this basis, it can be seen that the MOSFET has valuable application as a highly controllable switching device.

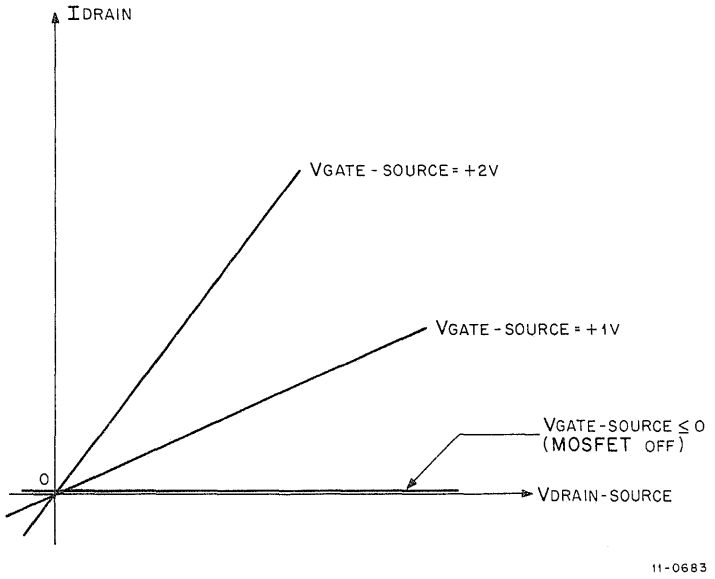


Figure A-2 Drain Characteristics of a MOSFET

A.3 THE MOSFET AS A MEMORY

The discussion thus far has considered the MOSFET as a static device; that is, the voltages applied to the device change very little, if at all, with respect to time during a given state of conductance. However, a MOSFET can also be considered a parallel-plate capacitor in which the gate electrode and the channel are the plates, and the metal-oxide layer is the dielectirc. Given this consideration, a MOSFET can be likened to a capacitive node, where for a given application of gate voltage, the current density is greatest at the source end of the channel and decreases to zero at the drain end. The time constant of this capacitive charge is of relatively long duration, up to 1 ms in most cases, due to the inherent high impedance of the MOSFET. This gate charge bears a linear relationship to applied gate voltage, so that, for a given application of gate voltage, a known capacitive charge can be stored. It can be seen, therefore, that the gate voltage controls the source-to-drain charge density. The important aspect for MOSFET memory application is that this source-to-drain charge determines, for a given source-to-drain voltage, the potential current flow if the drain is an open circuit.

In the dynamic MOSFET random access memory (RAM), the existence or non-existence of this capacitive charge is used to designate binary data; i.e., logic 1 or logic 0, respectively. The dynamic MOSFET RAM is based on the relatively simple 3-transistor memory cell shown in Figure A-3. For the purpose of describing circuit operation in Figure A-3, consider that in a P-Channel MOS IC network, logic 0 is typically - 1V, and logic 1 is +19V. To write data in the cell, a voltage corresponding to the data to be written is placed on the WD line and the WS line is forced to +19V. As a consequence, Q3 conducts and the capacitance C associated with the circuit is charged to

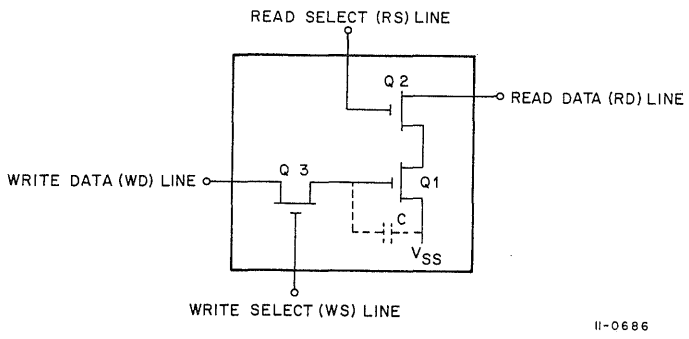


Figure A-3 Basic Dynamic MOS Storage Cell

the potential of the WD line. WS is then returned to 1V and the charge is retained in the cell as a potential at the drain of Q1.

To read from the cell, logic 1 is asserted, first on the RD line, then on the RS lime. This action causes Q2 to conduct. If a logic 1 is stored by virtue of the current potential at the drain of Q1, that potential will discharge on the RD line through Q2, forcing the RD line to logic 0. If a logic 0 is stored, the RD line will remain at logic 1.

The structure of the total 2-dimensional, integrated RAM array built from these cells provides logic for maintaining validity of stored data by periodically reading the content of each cell and writing the data read back into the cell. In addition, logic integrated to the RAM also provides for cell precharging prior to reading or writing.

The MOSFET RAM has a large operational advantage over the more conventional bipolar memory; i.e., power consumption. This advantage is apparent in both operating and standby power consumption. Operating power for the MOSFET RAM is nearly 1/10 of that required by the bipolar RAM, and standby power is more than 1/100 of the equivalent bipolar power consumption.

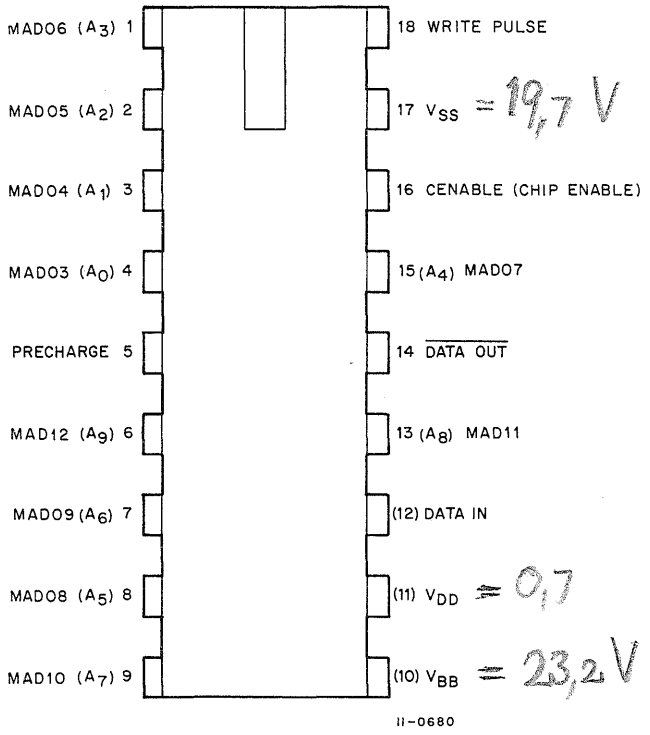
APPENDIX B
INTEGRATED CIRCUIT DESCRIPTIONS

This appendix contains descriptions of integrated circuits used only in the M8110, M8111, or G401 modules. Descriptions of other integrated circuits used throughout the PDP-11/45 System, as well as in the MS11 Semiconductor Memory System, are provided in Appendix A of the *PDP-11/45 System Maintenance Manual.*

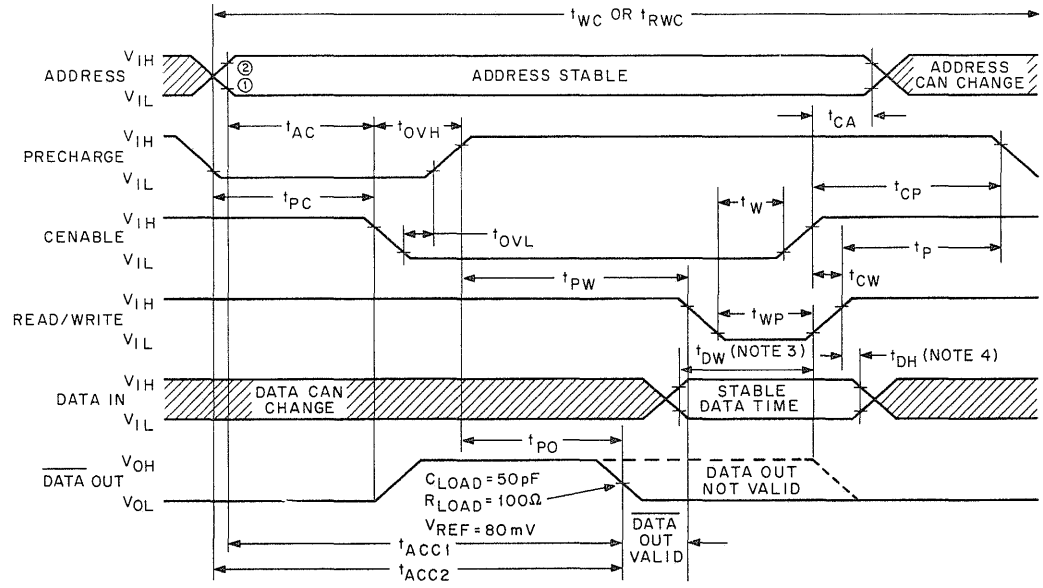
1103 RANDOM ACCESS 1024-BIT MEMORY

The 1103 random access 1024-bit dynamic metal-oxide semiconductor (MOS) memory is an MSI circuit characterized by high speed and extremely low power dissipation. The circuit is organized as a 1024 X 1-bit memory with integral address decoding, OR-tie capability at the outputs, and integral refresh logic. Data, once written, is read non-destructively. Refreshing of all 1024 bits in a circuit is accomplished in 32 read cycles, which are required every 2 ms. Data written into an 1103 memory is inverted when read so that a high, when written, is read as a 0 current, and a low, when written, is read as 0.9 mA (typical).

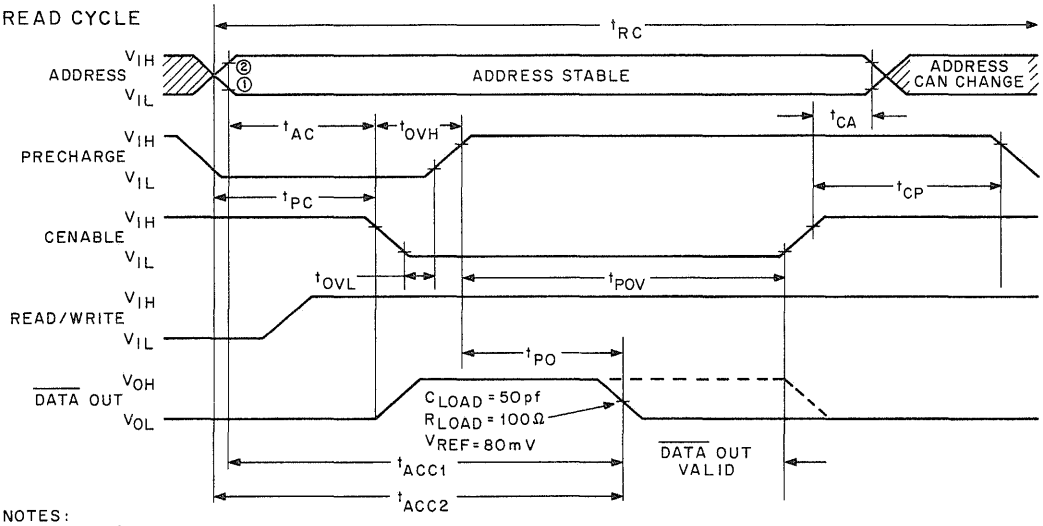
With reference to the block diagram and timing diagrams, access begins T_{AC} before the negative transition of CENABLE. During this period, PRECHARGE is active, and the address becomes stable in row and column decoders. After the CENABLE transition, the contents of the 32 cells along the selected row are written into the 32 on-chip refresh amplifiers, one of which is required for each column in the array. At the positive transition of PRECHARGE, the contents of the refresh amplifiers are written back into their respective columns, and the output appears T_{PO} later. T_{PW} after the positive edge of PRECHARGE, new data on the data input lead may be written into the selected cell, using a READ/WRITE pulse of minimum duration T_{WP}.



WRITE CYCLE OR READ/WRITE CYCLE



READ CYCLE



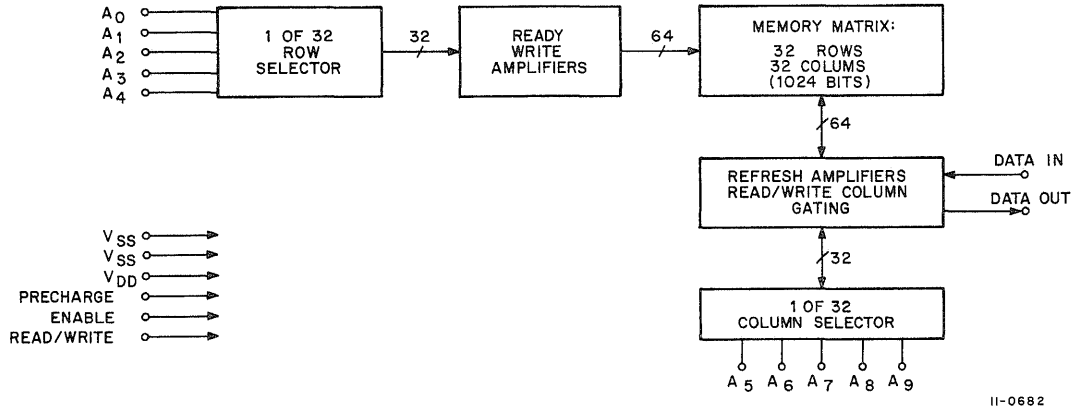
NOTES:

① V_{DD} = 2V
② V_{SS} = 2V
} t_t is defined as the transitions between these two points.

3. t_{DW} is referenced to point ① of the rising edge of chip enable or read/write, which ever occurs first.

4. t_{DH} is referenced to point ② of the rising edge of chip enable or read/write, which ever occurs first.

11-0859



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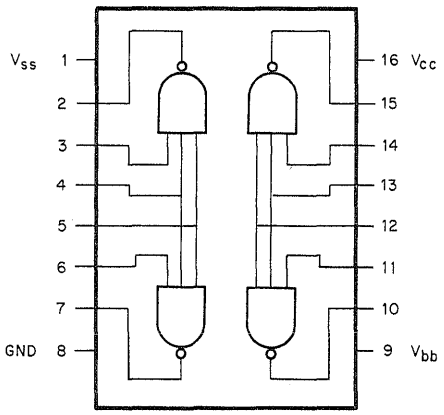
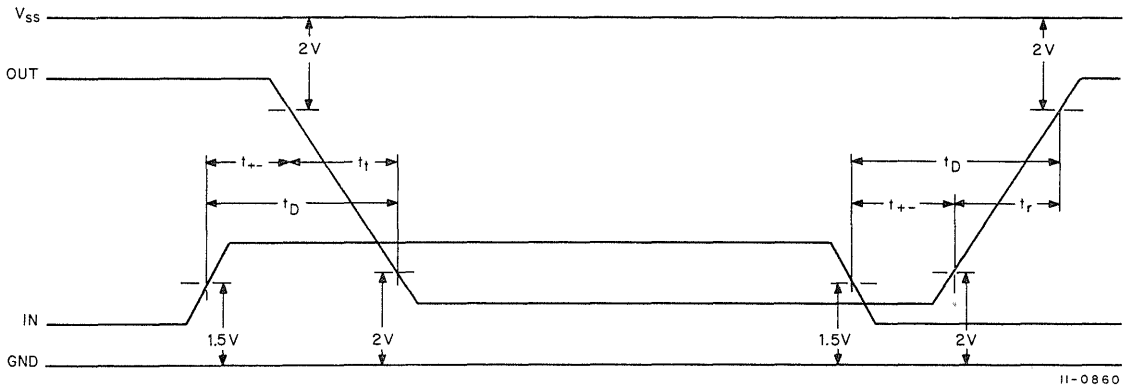
3207 QUAD 3-INPUT NAND TTL/MOS LEVEL SHIFTER

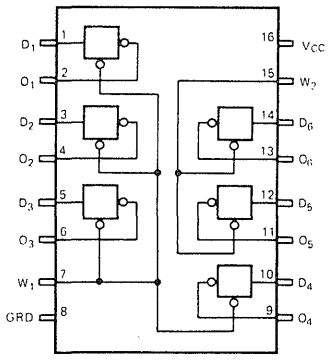
The 3207 TTL/MOS level-shifting integrated-circuit NAND gate provides an operational interface between TTL control circuits and MOS data storage circuits. Each gate in a unit is enabled by the coincidence of three +3V input levels. Enabled output is +19V. Inputs are connected so that each group of two gates has two common inputs with one unique input for each gate. This connection scheme permits cascaded level-shifting logic structures which are conditioned in common by the coincidence of several control levels, with the output of each gate being enabled by a single input.

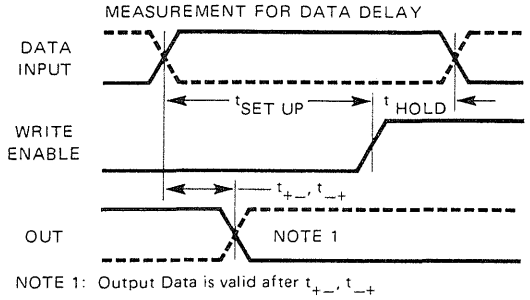




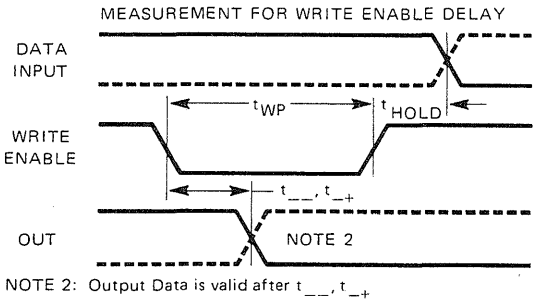
3404 HIGH SPEED HEX LATCH

The individual latching elements in the 3404 6-bit high-speed latching circuit are organized as separate 4-bit and 2-bit latches with each section having a common write line. This device is directly compatible with both DTL and TTL logic and provides an output sink capability of 10 mA minimum. The latches in this device can also act as high-speed inverters when the write input is held low.





NOTE 1: Output Data is valid after t_{+-}, t_{-+}



NOTE 2: Output Data is valid after t_{--}, t_{-+}

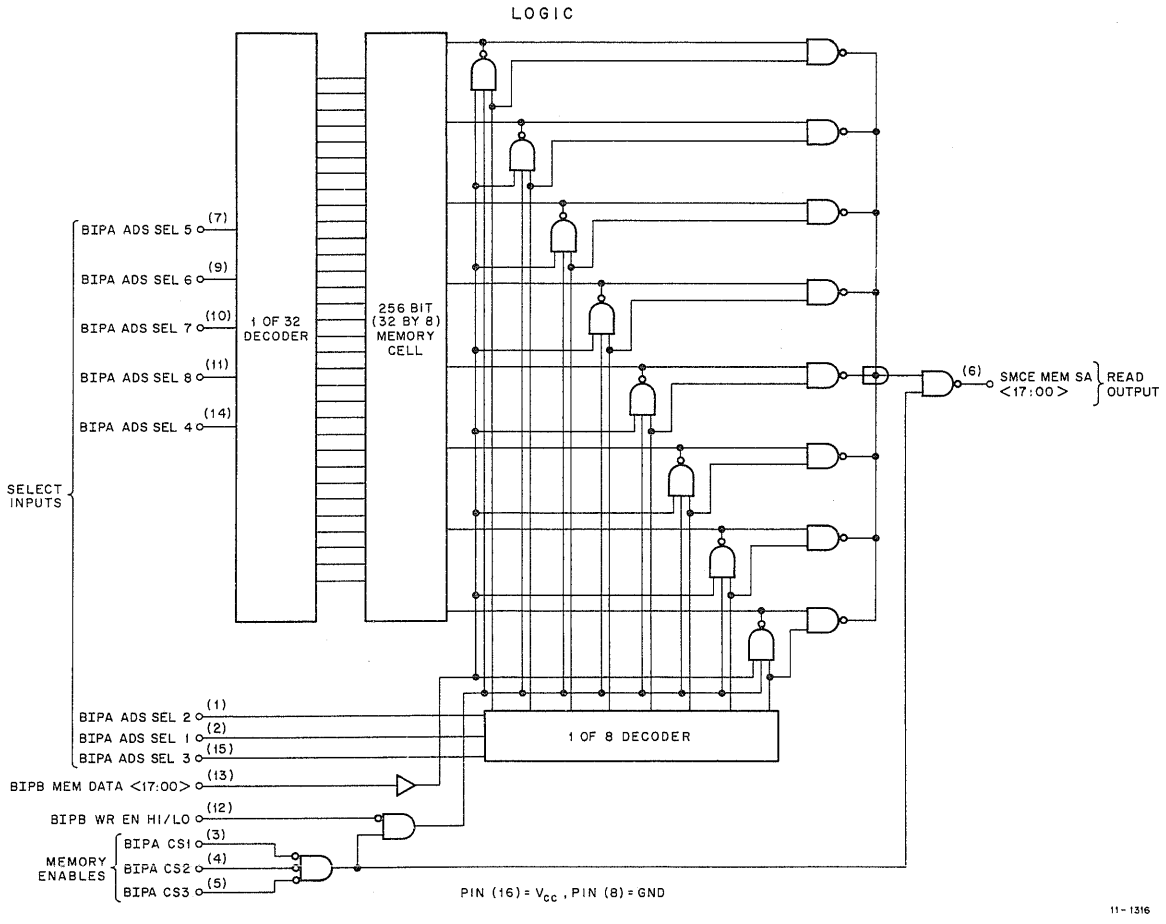
74200 BIPOLAR 256-BIT RANDOM ACCESS MEMORY

The 74200 integrated-circuit memory is a high-speed, fully decoded, static bipolar 256-bit RAM, organized as a 256 X 1-word memory. The circuit contains integral write and sense amplifiers with sense amplifier output being uncommitted collector output. Each circuit is addressed through the ADS SEL 1 to ADS SEL 8 inputs which select one of the 256 words. A circuit is enabled by placing all three CS inputs to logic 0. If the WR EN HI/LO (write enable) is at logic 0, the data at pin 13 is written into the addressed word in the complementary form. When WR EN HI/LO returns to logic 1, the data that was written can be read out. However, a bit as read is the complement of the same bit as written. The figure below shows the functional logic for one bit (a single IC on the M8111 module). Pin numbers are shown in parenthess.

RATINGS

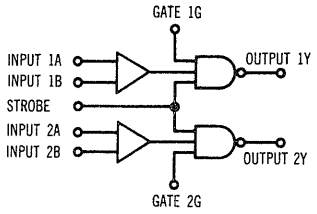
Tri-State Drive:

I_{OH}–High Level ON @ V_{OH}	-10 mA (min)	Input load factor	0.67
Output OFF @ V_{off}	±40 μA (max)	P_T (typical)	510 mW
I_{OL} –Low Level ON @ V_{OL}	16 mA (min)	Access Time (typical)	40 ns
V_{OH} minimum @ I_{OH}	2.4 V	Enable Time (typical)	20 ns
V_{off} (forced)	0.4 to 2.4 V	Sense Recovery Time (typical)	30 ns
V_{OL} maximum @ I_{OL}	0.4 V	Write Pulse Width (typical)	20 ns



75107/75108 DUAL-LINE RECEIVERS

The 75107 and 75108 dual-line receivers are linear integrated circuits consisting of two independent channels per circuit. Each receiver channel is formed by a differential input stage, a level shifting stage, and a TTL NAND gate output stage. The 75107 NAND gate stage provides the familiar totem pole output; the 75108 provides an open collector output at the NAND gate stage for wire-ORing.



TYPICAL CHARACTERISTICS		DIFFERENTIAL INPUT VOLTAGE	HIGH-LEVEL INPUT CURRENT	MAXIMUM COMMON-MODE INPUT VOLTAGE RANGE	TOTAL POWER DISSIPATION	PROPAGATION DELAY TIME (DIFFERENTIAL INPUTS)
		mV	μA	V	mV	ns
75107	DUAL LINE RECEIVER WITH (TTL) GATE OUTPUT	3	30	±3	134	17
75108	DUAL LINE RECEIVER WITH (OPEN-COLLECTOR) GATE OUTPUT	3	30	±3	134	19

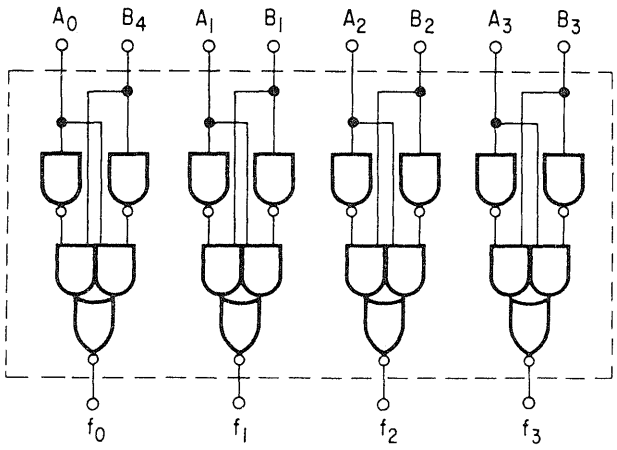
11-1074

8242 EXCLUSIVE-NOR 4-BIT DIGITAL COMPARATOR

The 8242 digital comparator circuit consists of four independent exclusive-NOR gates with each gate structure having an open collector output to permit multiple bit comparisons. A 4-bit comparator network is formed by connecting the independent outputs; such a network is easily expanded by cascading the outputs.

TRUTH TABLE

A	B	f
0	0	1
1	0	0
0	1	0
1	1	1



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